UNIVERSIDADE FEDERAL DO PARÁ
INSTITUTO DE TECNOLOGIA
PROGRAMA DE PÓS GRADUAÇÃO EM ENGENHARIA ELÉTRICA

PERFORMANCE EVALUATION OF ROBUST PARAMETRIC CONTROL STRATEGIES APPLIED ON SUPPRESSION OF OSCILLATIONS EFFECTS DUE TO CONSTANT POWER LOADS IN MULTI-CONVERTER BUCK-BUCK SYSTEMS

KEVIN EDUARDO LUCAS MARCILLO

DM: 21/2018

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Dissertação submetida à banca examinadora do programa de Pós-Graduação em Engenharia Elétrica da UFPA para obtenção do Grau de mestre em Engenharia Elétrica na área de Sistemas de Energia

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AUTOR: KEVIN EDUARDO LUCAS MARCILLO

DISSERTAÇÃO DE MESTRADO SUBMETIDA À AVALIAÇÃO DA BANCA EXAMINADORA APROVADA PELO COLEGIADO DO PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA DA UNIVERSIDADE FEDERAL DO PARÁ E JULGADA ADEQUADA PARA OBTENÇÃO DO GRAU DE MESTRE EM ENGENHARIA ELÉTRICA NA ÁREA DE SISTEMAS DE ENERGIA.

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DEDICATION

Dedico este trabajo primeramente a Dios y la Virgen María por haberme bendecido en este camino, darme una gran familia, brindarme salud y fuerza para poder seguir adelante.

Les dedico este trabajo también a mis padres, Jasmin Marcillo y Juan Carlos Lucas, por ser el pilar fundamental en mi vida, por ser mi ejemplo a seguir, por motivarme, por creer en mí en todo momento, y por haberme enseñado desde pequeño la importancia y valor del estudio.

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MUITO OBRIGADO

THANK YOU SO MUCH

MUCHAS GRACIAS

Epigraph

"Imagination is more important than
knowledge. Knowledge is limited. Imagination encircles the world."

Albert Einstein

"There is nothing either good or bad, but
thinking makes it so."

Hamlet Shakespeare

"Science is but a perversion of itself unless it
has as its ultimate goal the betterment of humanity."

Nikola Tesla

CONTENS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

PWM	Pulse Width-Modulation
CPL	Constant Power Load
SMC	Sliding mode control
DC	Direct Current
RPC	Robust Parametric Control
LP	Linear Programming
PID controller	Proportional-Integral-Derivative controller
ISE	Integral Square Error
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
CPP	Classical Pole-Placement
VMC	Voltage Mode Control
PMC	Power mode control
CKR	Control based on Kharitonov’s Rectangle
CCS	Control based on Chebyshev’s Sphere
ZOH	Zero-order hold
SISO system	Single-Input Single-Output system
LMI	Linear Matrix Inequality

RESUMO

Conversores chaveados são sistemas amplamente utilizadas em aplicações industriais. Tais sistemas operam via controle em malha fechada e, dessa forma, os aspectos de estabilidade e desempenho em malha fechada devem ser assegurados pelo projetista. Recentemente, o emprego de sistemas com múltiplos conversores vem se tornando comum em uma ampla gama de aplicações. A interação entre os sistemas de controle os múltiplos conversores pode levar o sistema a operar com reduzidas margens de estabilidade ou com um baixo desempenho dinâmico. Portanto, a estabilidade de um sistema com conversores operando em cascata é uma grande preocupação para aplicações reais. A instabilidade em sistemas em cascata pode ocorrer devido à carga de potência constante (CPL), que é um comportamento dos conversores quando se encontram regulados. As CPLs exibem comportamento de resistência negativa incremental, causando um alto risco de instabilidade em conversores interligados. Dessa forma, a mitigação desse problema é uma questão importante no projeto da fonte de alimentação comutada de múltiplos estágios, de modo a garantir a estabilidade de todo o sistema. No entanto, algumas dificuldades estão presentes além da CPL, por exemplo, não linearidades fortes, devido à presença do elemento indutivo, além das incertezas em relação aos valores nominais dos componentes discretos que compõem o sistema. Neste trabalho é realizado um estudo experimental do desempenho das metodologias de controle robusto paramétrico aplicadas ao problema de mitigar o efeito adverso de cargas do tipo CPL, em um sistema com dois conversores buck operando em cascata (sistema buck-buck). Vários testes foram desenvolvidos utilizando tanto uma planta experimental quanto via simulação computacional em Matlab/ Simulink, quando o sistema multiconversor buck-buck é submetido a uma variação de potência. Os resultados mostram o melhor desempenho das metodologias propostas.

Palavra-chave: sistema multiconversor; controle robusto paramétrico; CPL; variação paramétrica; teorema de estabilidade de kharitonov; Teorema de Chebyshev.

ABSTRACT

Multi-converter electronic systems are becoming widely used in many industrial applications; therefore, the stability of the cascaded system is a big concern to real-world power supplies applications. Instability in cascaded systems may occur due to the constant power load (CPL), which is a behavior of the tightly regulated converters. CPLs exhibit incremental negative resistance behavior causing a high risk of instability in interconnected converters; therefore, the mitigation of this problem is an important issue in the multiple-stage switched mode power supply design. Thus, it is important to guarantee stability of the whole system. However, some difficulties remains besides the CPL, e.g., non-linearities due to the inductive element and uncertainties due to imprecision of mathematical models and/or variation of nominal values of the discrete elements that compose the DC/DC buck converter. Aiming to evaluate the performance of the proposed robust methodologies in this work to mitigate the instability problem caused by a CPL, several tests were developed by using an experimental plant and Matlab/Simulink, when the multi-converter buck-buck system is subjected a variation of power reference. The results show the improved performance of the proposed methodologies.

Key-word: multi-converter system; robust control; robust parametric control; constant power load; parametric variation; buck converter; kharitonov stability theorem; chebyshev theorem.

CHAPTER 1
INTRODUCTION

1.1 STATE-OF-THE-ART

Nowadays, DC-DC converters are increasingly used in industrial applications due to their simplicity in structure, high power efficiency, low cost and high reliability [1], [2]. Some modern industries, whose processes demand high dynamic performance, have applied different types of converters for applications such as in variable speed DC motor drivers [3], renewable energy systems [4]-[6], transportation systems [7], [8], hybrid energy storage system [9], [10], communications systems [11]. In several of these applications, converters are controlled by switching through Pulse Width-Modulation (PWM) to transfer power from a power source to loads having a constant power characteristic. Because of switching, the converter converters have some inherent nonlinear behaviors [12], [13]. Therefore, it is a challenging task to ensure the stability, transient performance and higher efficiency of such converters [13]. The non-linear behavior, due to switching operation, has been usually neglected while designing the converter [2]. One important converter topology is the DC-DC buck converters where the required output voltage is lower than the source voltage. DC-DC buck converters are typically dynamical nonlinear systems and their control problems are well acknowledged as a challenging issue [14]-[16]. The main reasons are: load variations, power source variations, inevitable parameter uncertainties and exogenous disturbances. All these uncertainties could lead to instability and performance degradation.

On the other hand, cascaded converters have a basic configuration that consists of two converters in series connection, where the first is a source converter while the second one is a load converter. The source converter maintains a regulated dc voltage on the intermediate bus, and the load converter convert the intermediate bus voltage to tightly regulated outputs for the

next system stage or load. When a converter tightly regulates its output, it behaves as a Constant Power Load (CPL), so load converter acts as a CPL when tightly regulated [18] and its dynamic response is faster than the dynamic response of the source converter. If the source converter is faster than the load converter, then it will compensate for disturbances and will regulate its output before the feedback loop of the load converter reacts to disturbances. Therefore, the load converter will not act as a perfect CPL for the feeding converter [19]-[25]. Different from a resistive load, CPL is a nonlinear load with variable negative impedance characteristics, i.e. the input current increases/decreases with a decrease/increase in its terminal voltage [19]-[25]. Because of the negative impedance characteristics of CPL, the system may become unstable, which may lead the system into oscillation or failure, and stress or damage the system equipment when feeding a CPL [21]-[25]. For this issue, CPLs are receiving more attention of researchers to give solutions aiming at to cancel or compensate the instability caused by CPL.

1.2 MOTIVATION AND JUSTIFICATION

Traditionally, the stability analysis and controller design of cascaded dc-dc converters is carried out by using the impedance criterion applied to averaged and linearized models [23]-[26]. The load converter under a tight control is conventionally modeled constant power load (CPL) for stability analysis or for controller design [23]-[26].

In order to mitigate the destabilizing effect of CPL, several methods have been proposed, such as passive and active damping [27]-[29], Lyapunov redesign control [8], nonlinear feedback linearization [30]-[33], sliding mode control (SMC) [34], [35], fuzzy control [36], and robust control [37], [38]. In addition, the robust parametric control methodology can be found in the literature to control dc-dc power converters [39]-[41].

The controller design is usually based on the linear approximation of nonlinear dynamics of the converter. Linear controllers are usually used to regulate the output voltage

[14], [42] of converters. However, conventional controllers may experience a sensible performance deterioration under varying operating conditions [39]-[41]. In order to assure robustness against parameter uncertainties, linear controllers must be designed by using robust control theory. Therefore, the controller can be designed to cope with a pre-specified range of parameter uncertainties, load variations, or a wide variation of operating points. Besides of that, the performance of the DC-DC converters is also affected by external disturbance, which may cause instability that usually appear due to the measurement noises [40]-[41]. Therefore, the controller design process must ensure the performance robustness.

In research on dynamic systems with parametric uncertainties, the techniques that deal with this problem have been studied extensively over the last 40 years [42], [43]. In this context, control strategies, which aim to implement adaptive, predictive and fuzzy control algorithms, have been widely studied for the resolution of control problems of systems with parametric uncertainties. However, these strategies, being able to offer efficient and satisfactory results, can make the implementation and operation of the process more complex [44].

Within the context of solutions for process control, one of the areas that have received great research efforts from the scientific community is Robust Parametric Control (RPC) Theory. Such classes of robust control approaches take into account the available apriori information about possible range of plant´s parameters, around their respective nominal values [45]. The RPC gained greater attention from academia since the 1980s because of Kharitonov's work, who developed the so-called seminal Kharitonov stability Theorem. Among the several methods of solution to the problem of controlling plants with parametric uncertainties, in the present work, are highlighted the use of Linear Programming (LP) approach [46] and the Chebyshev Theorem [47]. These methods, when combined, serve to design optimal and robust controllers.

In this work, a design trend is presented for Proportional-Integral-Derivative (PID) controllers' family based on parametric robust control theory. The controller designed is applied to a source converter in a multi-converter system to suppress of oscillations effects due to constant power loads in multi-converter buck-buck systems, aiming to reduce the control effort when the system is operating outside its nominal operating point. The motivation arises from the difficulty of relating parametric robust control theory to conventional design methods. In conventional methods, the goal is to design a controller with fixed parameters from a plant with fixed parameters too. However, robust parametric control presents a different form of controller development, in which the modelling of the systems is developed with the plant parameters represented by real intervals (not fix). From the method presented in [46], it is possible to develop controllers designed for an interval domain and still with fix parameters. The reason for choosing the controllers of the PID family is justified by the fact that it is the most popular controller in the industrial environment [48]. In [46] and [49], a linear programming approach is used to provide necessary conditions on the fixed-order controller design for robust stability of the closed-loop systems. In [40], the design of a robust controller via linear programming is presented in comparison to a conventional design technique applied to the output voltage control of a DC-DC buck converter. In these works, only linear programming approach is used to solve the optimization problem proposed for tuning of the controllers parameters.

Theoretical contributions of the RPC combined with conventional control techniques emphasize the importance of the RPC in different current applications such as drones [50], industrial processes [51], [39] and power systems [52]. Therefore, in this work a control strategy is proposed combining the linear programing approach [46] with Chebyshev Theorem [47], to optimize the parameters of an interval robust controller, providing better control performance. In addition, robust controller design is presented with robust stability guaranteed according to Kharitonov Theorem.

1.3 DEFINITION OF OBJECTIVES

1.3.1 General Purpose

To evaluate robust control strategies applied to a multi-converter buck-buck system in order to stabilize the oscillations of whole system caused by a constant power load.

1.3.2 Specific Objective

- To analyze the dc-dc buck converter dynamics by feeding a constant power load.
- To carry out an experimental and simulation evaluation of robust control strategies applied to the multi-converter buck-buck system, when it is subjected to a variation of power reference.
- To carry out the evaluation of the Integral Square Error (ISE) cost function, in order to verify the robustness and performance of the control strategies evaluated, when the multi-converter buck-buck system is subjected to a variation of power reference.

1.4 OUTLINE

The remainder of this work is organized as follows: Chapter 2 presents a brief review about the multi-converter buck-buck system; Chapter 3 presents a brief review about parametric robust control background in addition to the design methodologies for robust controllers. Chapter 4 presents the methodologies developed in this study, describing the simulation environment, as well as the experimental environment, and then the experiments to be performed in this work are described. Chapter 5 presents an assessment of the simulation results and experimental data. Finally, Chapter 6 presents the final considerations of the dissertation and recommendations for future works.

CHAPTER 2

SYSTEM DESCRIPTION

2.1 INTRODUCCTION

In a DC network, the operation of DC-DC power converters is similar to transformers in AC networks, that is, increase or decrease the input voltage, generating an output power equal, in ideal conditions, without the use of external power. These converters present six main topologies: *Buck, Boost, Buck-Boost, Cuk, Sepic e Zeta*; or some derivations of them [12]. In addition, they can be unidirectional, with only a conduction sense, or bidirectional, whose conduction sense can be reversed. According to architecture of the filters, it may be classified them according to their order [54].

Multi-converter cascading power systems are very common in most application in industry [3]-[11]. When a power converter tightly regulates its output, it behaves as a CPL [18]. CPLs have a negative incremental resistance, which tends to destabilize the power system [23]-[25].

In this chapter, the study system is presented. First for a buck converter, the topology, operation and conduction modes and dynamic are analyzed. Then the cascaded converter system is presented, analyzing its dynamics and instability issue due to CPL.

2.2 DC-DC BUCK CONVERTER

DC-DC converters are electronic devices that convert a direct voltage or a direct current value to a different level. This conversion can be obtained with the combination of an inductor and/or a capacitor, and a solid-state device operating in the high frequency switching mode. In the buck converter case, also called Step-Down or voltage drop, the output has a lower voltage

than the input voltage. A typical topology of buck converter shown in Fig. 2.1. d is switch, L is inductance, C is capacitance, D_1 is freewheel diode, R_L is load resistance. i_L is the current of inductance L , V_i is input voltage, v_c is output capacitor voltage.

Buck converter operation can be analyzed in two alternate states for each period of the digital control signal [53],[54]. First state occurs when MOSFET, Q_1, is "on" and diode, D_1, is "off", causing the energy transfer from the source to the inductor, capacitor and load, charging the inductor and capacitor, as well as feeding the load. In second stage, Q_1 is "off", and D_1 is "on", so that the inductor current behaves as the power source for the load, causing its gradual discharge. When inductor current becomes smaller than drained by the load resistor, capacitor starts a discharge to supply it. At the end of a period, Q_1 is "on" and the cycle is restarted. The time in which Q_1 is "on" or "off" is controlled by PWM.

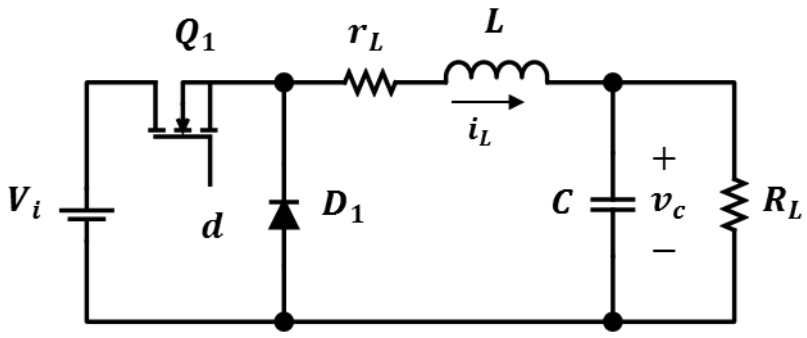

Figure 2.1. Buck converter topology.

2.2.1 Conduction modes of Buck Converter

According to inductor current variation, buck converter can present three different conduction modes: continuous, discontinuous and critical conduction [53], [54].

In continuous conduction mode, Buck Converter assumes two states per switching cycle. First, ON state is when Q_1 is “on” and D_1 is “off”, inductor current, i_L, flows from the input source, V_i, through Q_1 and to output capacitor and load resistor combination. During the ON state, the voltage applied across the inductor is constant and increases linearly. Second,

OFF state is when Q_1 is "off" and D_1 is "on". During the OFF state, the magnitude of the voltage applied across the inductor is constant. Maintaining the same polarity convention, this applied voltage is negative (or opposite in polarity from the applied voltage during the ON time). Hence, the inductor current decreases during the OFF time. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuits during each state. The circuit diagram for each of the two states is shown in Fig. 2.2. The increase and decrease in inductor current, during T_{ON} and T_{OFF} respectively, are illustrated in Fig. 2.3.

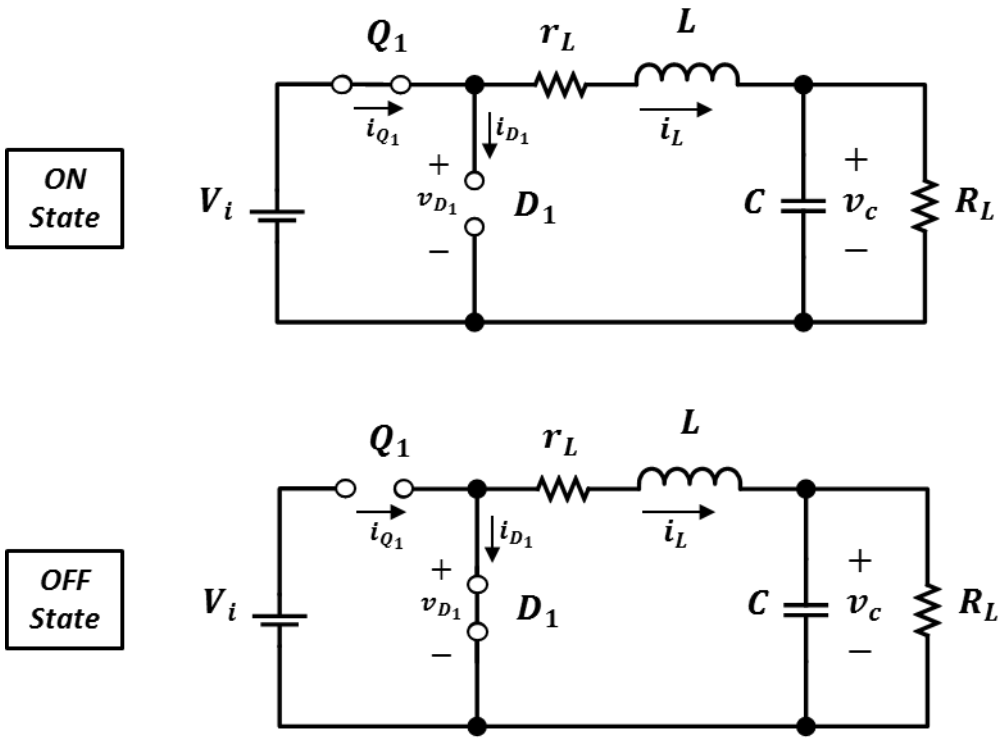

Figure 2.2. Buck Power Stage States.

The ON state duration is $D = \frac{T_{ON}}{T_S}$ where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, T_s. The OFF state duration is called T_{OFF} where $T_{OFF} = (1 - D)T_s,\ D' = (1 - D)$. Since there are only two states per switching cycle for continuous mode. These times are shown along with the waveforms in Fig. 2.3.

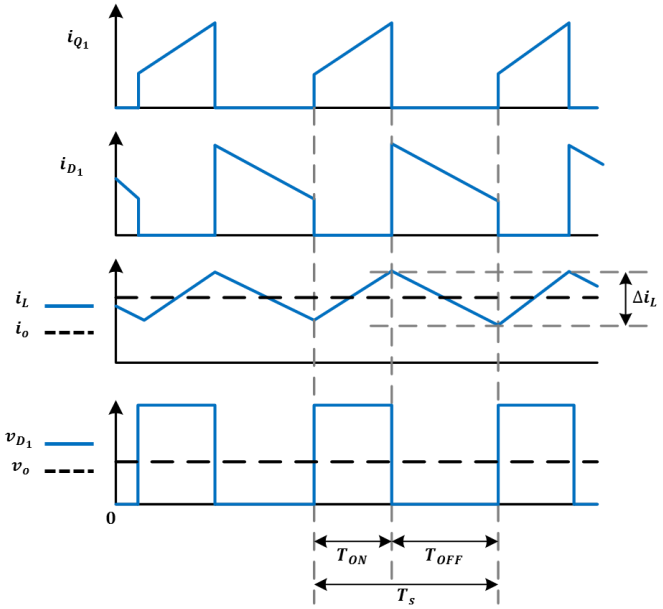

Figure 2.3. Typical waveforms for Buck Power Stage States.

In Discontinuous Conduction Mode (DCM), inductor current is zero for a portion of switching cycle due to the reduction of the load current below the critical current level. In a (nonsynchronous) buck power stage, if the inductor current attempts to fall below zero, it just stops at zero (due to the unidirectional current flow in D_1) and remains there until the beginning of the next switching cycle. A power stage operating in discontinuous conduction mode has three unique states during each switching cycle as opposed to two states for continuous conduction mode. The load current condition where the power stage is at the boundary between continuous and discontinuous mode is shown in Fig. 2.4. This is where the inductor current falls to zero and the next switching cycle begins immediately after the current reaches zero.

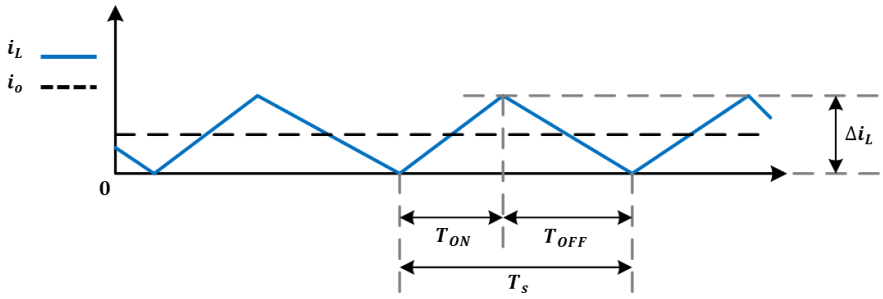

Figure 2.4. Boundary between Continuous and Discontinuous Mode.

Further reduction in output load current puts the power stage into discontinuous conduction mode. This condition is illustrated in Fig. 2.5.

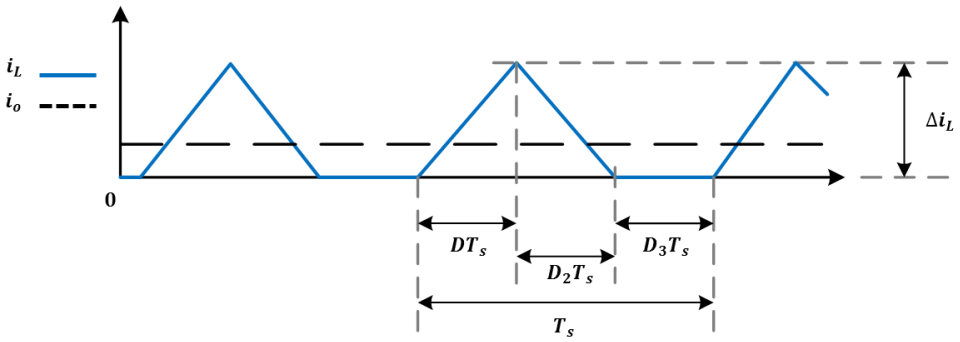

Figure 2.5. Discontinuous Current Mode.

The power stage assumes three unique states during discontinuous current mode operation. First, ON state is when Q_1 is "on" and D_1 is "off". Second, OFF state is when Q_1 is "off" and D_1 is "on". And finally, IDLE state that is when both Q_1 and D_1 are "off". The first two states are identical to those of the continuous mode case and the circuits of Fig. 2.2 are applicable except that $T_{OFF} \neq (1 - D)T_s$. The remainder of the switching cycle is the IDLE state. In addition, dc resistance of the output inductor, output diode forward voltage drop, and power MOSFET ON-state voltage drop are all assumed to be small enough to omit.

ON state duration is $DT_s = T_{ON}$,where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, T_s. OFF state duration is $T_{OFF} = D_2T_s$. The IDLE time is the remainder of the switching cycle and is given as $D_3T_s = T_s - T_{ON} - T_{OFF}$. These times are shown with the waveforms in Fig. 2.6.

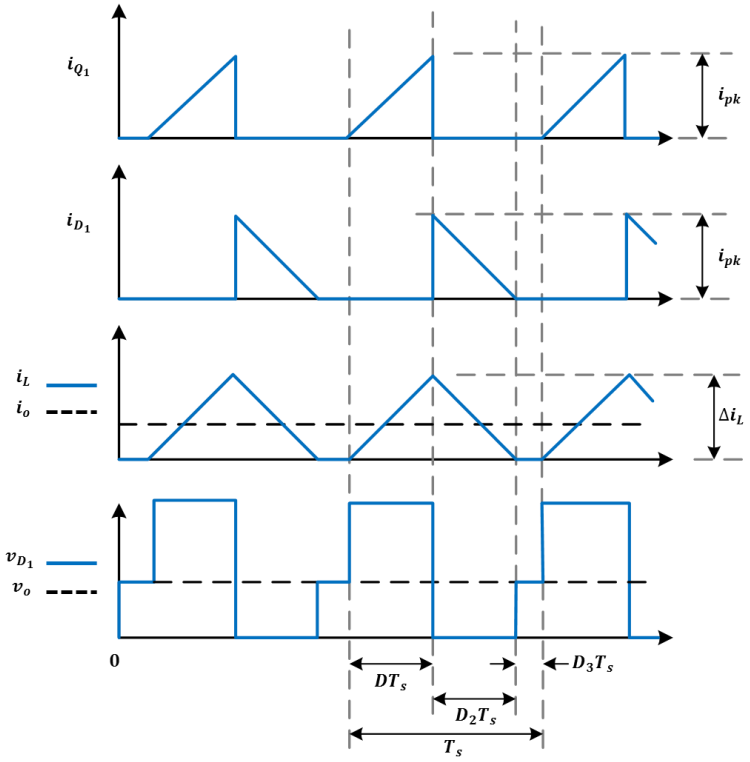

Figure 2.6. Discontinuous-Mode Buck Power Stage Waveforms.

where i_{pk} is the peak inductor current.

It should be noted that the buck power stage is rarely operated in discontinuous conduction mode in normal situations, but discontinuous conduction mode will occur anytime the load current is below the critical level.

In critical conduction mode, inductor current reaches the zero value at the exact moment of a new switching cycle, immediately increasing again. Thus, a buck power stage can be designed to operate in continuous mode for load currents above a certain level usually 5% to 10% of full load. Usually, the input voltage range, the output voltage and load current are defined by the power stage specification. This leaves the inductor value as the design parameter to maintain continuous conduction mode [54].

2.2.2 Dynamic of Buck Converter

As shown in Fig. 2.1, the model of buck converter in Continuous Conduction Mode (CCM) can be written as follows:

$$\begin{cases} L\dfrac{di_L(t)}{dt} = d(t)V_i - v_c(t) - r_L i_L(t) \\ C\dfrac{dv_c(t)}{dt} = i_L(t) - \dfrac{v_c(t)}{R_L} \end{cases} \tag{2.1}$$

Considering the presence of energy storage elements in the circuit, the system modeling must be based on the differential equations that determine the behavior of its state variables, the voltage in the capacitor (v_c) and the current in the inductor (i_L), and its organization in state equations [55], and ($d(t)$) is the duty cycle. Due to the non-linearity introduced by static switching, the analysis can be divided into two different operation intervals for each period as discussed above in the continuous operation mode. Therefore, ON stage, when $0 \leq t \leq T_{ON}$, $i_C(t) = i_L(t) - i_{R_L}(t)$, $v_L(t) = V_i - v_c(t)$, and $d(t) = 1$. Thus for the ON stage, state equations are given by equations (2.2) and (2.3).

$$\frac{di_L(t)}{dt}_{ON} = -\frac{r_L}{L}i_L(t) - \frac{1}{L}v_c(t) + \frac{V_i}{L} \tag{2.2}$$

$$\frac{dv_c(t)}{dt}_{ON} = \frac{1}{C}i_L(t) - \frac{1}{R_L.C}v_c(t) \tag{2.3}$$

$$\begin{bmatrix} \dfrac{di_L}{dt} \\ \dfrac{dv_c}{dt} \end{bmatrix}_{ON} = \begin{bmatrix} -\dfrac{r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L.C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} V_i \tag{2.4}$$

For the OFF stage, when $T_{ON} \leq t \leq T_s$, $i_C(t) = i_L(t) - i_R(t)$, $v_L(t) = -v_c(t)$, and $d(t) = 0$. The state equations that represent this stage are shown below,

$$\frac{di_L(t)}{dt}_{OFF} = -\frac{r_L}{L}i_L(t) - \frac{1}{L}v_c(t) \tag{2.5}$$

$$\frac{dv_c(t)}{dt}_{OFF} = \frac{1}{C} i_L(t) - \frac{1}{R_L.C} v_c(t) \tag{2.6}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix}_{OFF} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L.C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i \tag{2.7}$$

Equations (2.4) and (2.7) represent the mathematical model in the state space of the buck converter in CCM. Therefore, the dynamic behavior of the converter can be approximated by a switching cycle as shown in equations (2.8) and (2.9),

$$T_s \cdot \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = d(t) \cdot T_s \cdot \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} + [1 - d(t)] \cdot T_s \cdot \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} \tag{2.8}$$

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L.C} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \frac{V_i}{L} \\ 0 \end{bmatrix} d(t) \tag{2.9}$$

Considering the practical interest of controlling the converter output by switching applied to gate of power transistor and defining the capacitor voltage as output of the system, $y(t)$, the transfer function for voltage control, described in (2.12), can be calculated by equation (2.11).

$$y(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{2.10}$$

$$\frac{V_c(s)}{D(s)} = C \cdot (sI - A)^{-1} \cdot B + D \tag{2.11}$$

$$\frac{V_c(s)}{D(s)} = \frac{{V_i}/{LC}}{s^2 + \left(\frac{1}{R_L.C} + \frac{r_L}{L}\right)s + \left(\frac{1}{LC} + \frac{r_L}{R_L \cdot L \cdot C}\right)} \tag{2.12}$$

2.3 CASCADED DC-DC BUCK CONVERTER SYSTEM

A multi-converter system comprised of cascaded converters have a basic configuration that consists of two or more converters in series connection, where the first is a source converter that maintains a regulated dc voltage on the intermediate bus while remaining are load converters that convert the intermediate bus voltage to tightly regulated outputs for the next system stage or load. In a cascaded buck converter system a large variety of dynamic and static interactions are possible and these can lead to irregular behavior of a converter, a group of converters or the whole system. A typical cascaded system with *N* DC–DC buck converters is shown in Fig. 2.7(A). Fig. 2.7(B) shows a generic configuration for voltage control for the k-th converter.

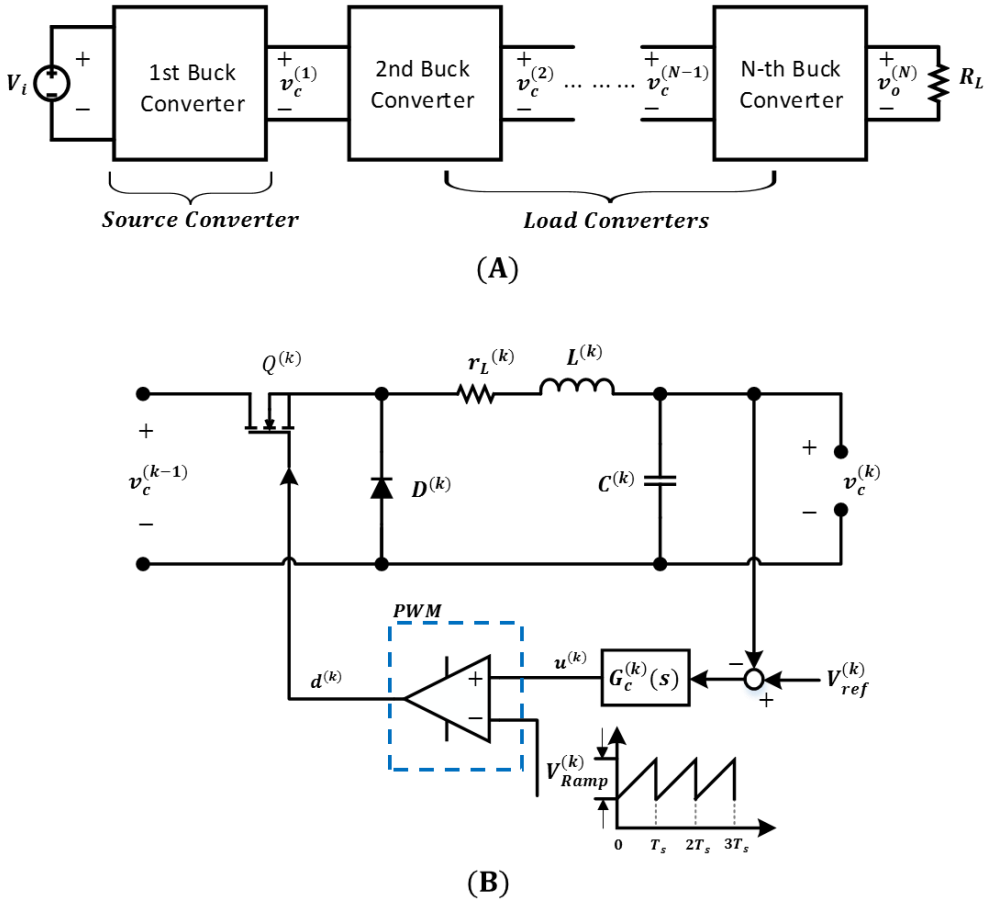

Figure 2.7. Buck Converter system in series connection: (A) Cascaded system with N-converter. (B) Voltage mode control for the k-th converter.

As mentioned earlier, when a load converter is tightly regulated and its switching operation frequency is faster than source converter, load converter behavior will be as a CPL. As a result, in CPL, input current increases when input voltage decreases, and vice versa. CPL approximation model describe the behavior at the input terminals of the load converter allows to capture its performance in a frequency range where its open-loop gain is high and an input voltage span where its controller is within its dynamic range.

2.3.1 Buck Converter with constant power load

Cascaded buck converter system and its representation with CPL are shown in Figs. 7.8(A) and 7.8(B), respectively. Source and load converter are in voltage control mode as shown in Figs. 7.8(C) and 7.8(D).

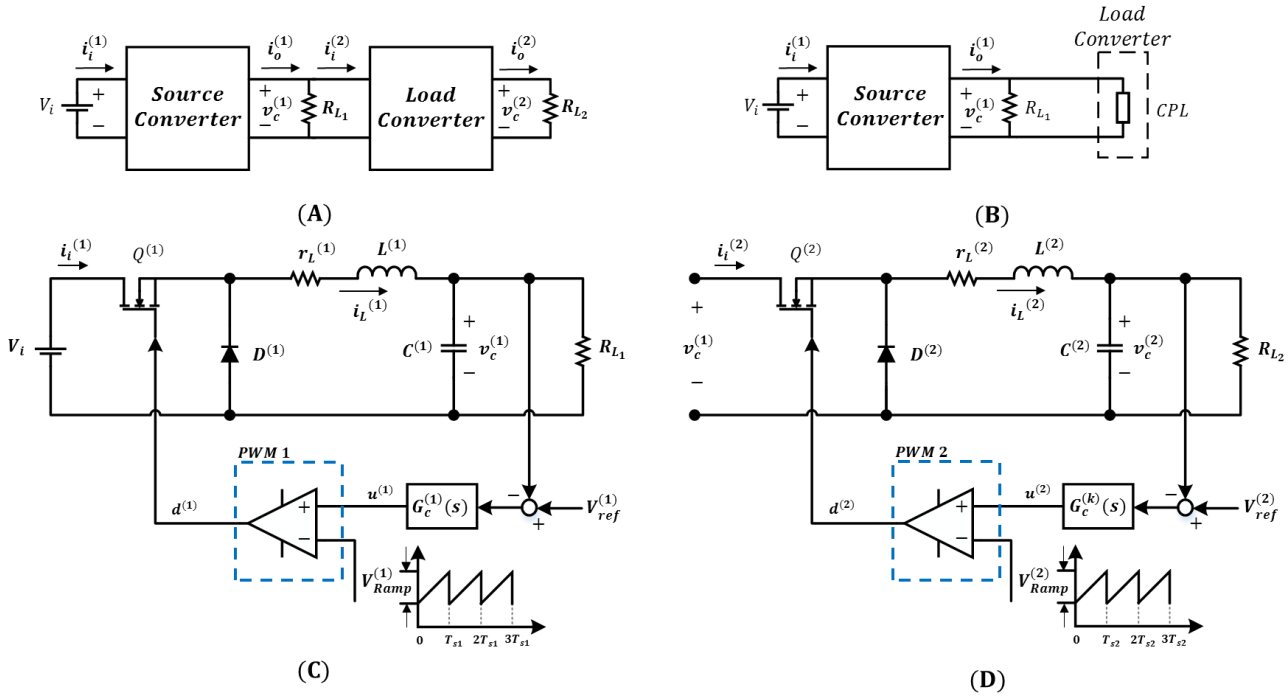

Figure 2.8. Cascaded buck converter with two power stages. (A) Diagram of the cascaded converters. (B) Source converter loaded by a CPL. (C) Voltage mode control for source converter. (D) Tight regulated load converter.

CPLs introduce interesting nonlinear behavior to conventional buck-converter dynamics but this behavior only exhibit above a certain voltage (see Fig. 2.9). Fig. 2.9 shows the input "V-I" characteristics of load converter. When the input voltage of the load converter, $v_c{}^{(1)}$, is

lower than $\left({v_c}^{(2)}/{d_{max}^{(2)}}\right)$, the load converter behavior will be as the resistive load. Therefore, in this range of operation, load converter will be operate in a constant resistor zone (CRZ). On the other hand, when ${v_c}^{(1)}$ is higher than $\left({v_c}^{(2)}/{d_{max}^{(2)}}\right)$, the load converter behavior will be as a CPL, thus, load converter will be operate in a constant power zone (CPZ).

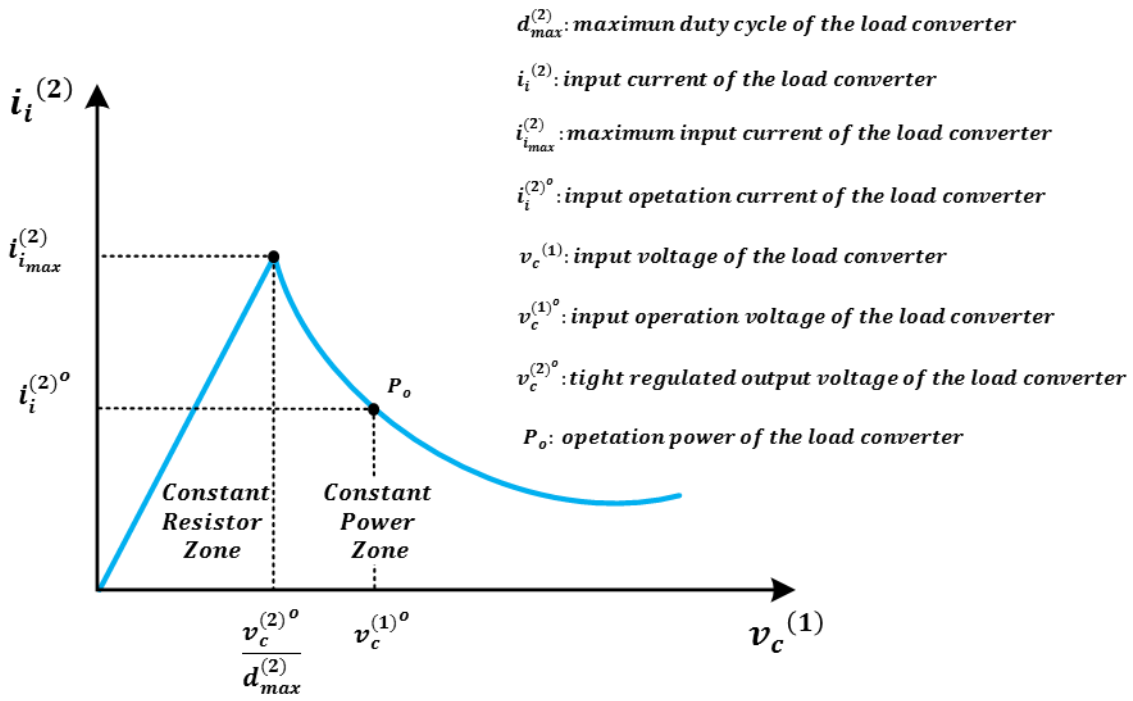

Figure 2.9. Input "V –I" characteristics of the CPL.

For a CPL, in order to maintain a constant power level, in load converter, input current increases when input voltage decreases, and vice versa, so the product of the input current and input voltage of the load converter $\left(\text{i.e., } P_o = i_i^{(2)} v_c^{(2)}\right)$ is a constant and the instantaneous value of the load impedance is positive $\left(\text{i.e., } {v_c^{(2)}}/{i_i^{(2)}} > 0\right)$. However, the incremental impedance is always negative (i.e., $\Delta V/\Delta I < 0$) due to once appearing any disturbance, thus operating point will leave from previous point and never return. This negative incremental

impedance has a negative impact on the power quality and stability of the system. The curve, in Fig. 2.10, shows the negative incremental impedance behavior of CPL.

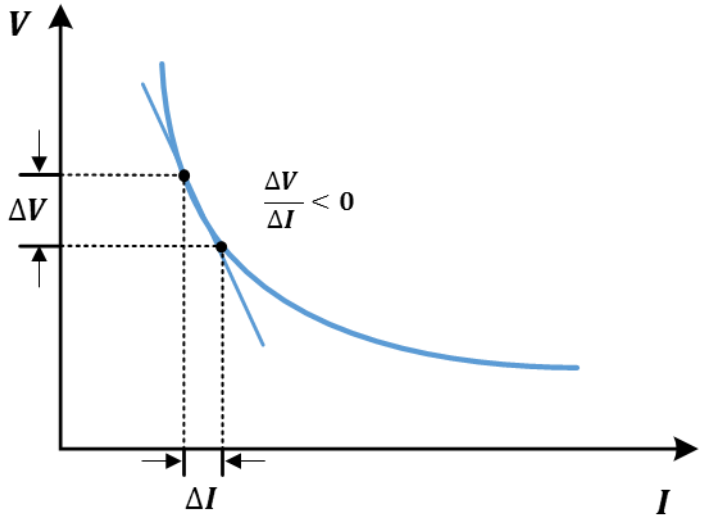

Figure 2.10. The negative incremental impedance behavior of CPL.

2.3.2 Instability in a DC-DC Buck Converter with constant power load

The system (see Fig. 8(B)) is used to show the instability of a dc-dc converter with a constant power load. To obtain the large-signal behavior of the load converter, the CPL is represented by a dependent current source, $i_{CPL}(t) = \frac{P_o}{v_c^{(1)}(t)}$, so the total instantaneous current drawn from source converter is given by

$$i_o^{(1)}(t) = \frac{v_c^{(1)}(t)}{R_{L_1}} + \frac{P_o}{v_c^{(1)}(t)} \tag{2.13}$$

$$i_o^{(1)}(t) = i_{R_{L_1}}(t) + i_{CPL}(t) \tag{2.14}$$

where, P_o in the output power of the converter that is constant.

Depending on switching of the source converter, the large-signal model of the converter in CCM can be obtained based on the following equations:

$$\begin{cases} \dfrac{di_L^{(1)}(t)}{dt} = -\dfrac{r_L^{(1)}}{L^{(1)}} i_L^{(1)}(t) + \dfrac{1}{L^{(1)}}\left(V_i - v_c^{(1)}(t)\right) \\ \dfrac{dv_c^{(1)}(t)}{dt} = \dfrac{1}{C^{(1)}} i_L^{(1)}(t) - \dfrac{1}{C^{(1)}}\left(\dfrac{v_o^{(1)}(t)}{R_{L_1}} + \dfrac{P_o}{v_c^{(1)}(t)}\right) \end{cases} \quad \text{When } 0 < t < d^{(1)}T_{s_1} \qquad (2.15)$$

$$\begin{cases} \dfrac{di_L^{(1)}(t)}{dt} = -\dfrac{r_L^{(1)}}{L^{(1)}} i_L^{(1)}(t) + \dfrac{1}{L}\left(-v_c^{(1)}(t)\right) \\ \dfrac{dv_c^{(1)}(t)}{dt} = \dfrac{1}{C^{(1)}} i_L^{(1)} - \dfrac{1}{C^{(1)}}\left(\dfrac{v_c^{(1)}(t)}{R_{L_1}} + \dfrac{P_o}{v_c^{(1)}(t)}\right) \end{cases} \quad \text{When } d^{(1)}T_{s_1} < t < T_{s_1} \qquad (2.16)$$

where $d^{(1)}\ and\ T_{s_1}$ are the duty cycle and switching period of the source converter, respectively. Using the state-space averaging method [14], [40], [41], the buck converter dynamic can be written as

$$\begin{cases} \dfrac{di_L^{(1)}(t)}{dt} = -\dfrac{r_L^{(1)}}{L^{(1)}} i_L^{(1)}(t) + \dfrac{1}{L^{(1)}}\left(V_i \cdot d^{(1)} - v_c^{(1)}(t)\right) \\ \dfrac{dv_c^{(1)}(t)}{dt} = \dfrac{1}{C^{(1)}} i_L^{(1)}(t) - \dfrac{1}{C^{(1)}}\left(\dfrac{v_c^{(1)}(t)}{R_{L_1}} + \dfrac{P_o}{v_c^{(1)}(t)}\right) \end{cases} \qquad (2.17)$$

Consider small perturbations in the state variables due to small disturbances in the input voltage and duty cycle

$$\begin{cases} V_i = \bar{V}_i + \tilde{V}_i \\ d^{(1)} = D^{(1)} + \tilde{d}^{(1)} \\ v_c^{(1)} = V_c^{(1)} + \tilde{v}_c^{(1)} \\ i_L^{(1)} = I_L^{(1)} + \tilde{i}_L^{(1)} \end{cases} \qquad (2.18)$$

where, $\bar{V}_i$, $D^{(1)}$, $V_c^{(1)}$, and $I_L^{(1)}$ are the average values of V_i, $d^{(1)}$, $v_c^{(1)}$ and $i_L^{(1)}$, respectively. Substituting (2.18) in (2.17) and neglecting the internal resistance of the inductor to simplify the calculations, the buck converter dynamic becomes

$$\begin{cases} \dfrac{d\tilde{\imath}_L^{(1)}}{dt} = \dfrac{1}{L^{(1)}}\left(\bar{V}_i \cdot \tilde{d}^{(1)} + D^{(1)}\tilde{V}_i - \tilde{v}_c^{(1)}\right) \\ \dfrac{d\tilde{v}_c^{(1)}}{dt} = \dfrac{1}{C^{(1)}}\left(\tilde{\imath}_L^{(1)}(t) - \dfrac{P_o\tilde{v}_c^{(1)}}{V_c^2}\right) \end{cases} \tag{2.18}$$

Note that the following approximation was made in (2.18), $\bar{V}_i \gg \tilde{V}_i$ and $V_c^{(1)} \gg \tilde{v}_c^{(1)}$.

The transfer functions of the system can be obtained from (2.18) as follows:

$$\begin{cases} G_1(s) = \dfrac{\tilde{v}_c^{(1)}(s)}{\tilde{d}^{(1)}(s)} = \dfrac{\bar{V}_i/_{LC}}{s^2 - \left(\dfrac{P_o}{CV_c^2}\right)s + \dfrac{1}{LC}} \\ G_2(s) = \dfrac{\tilde{v}_c^{(1)}(s)}{\tilde{V}_i(s)} = \dfrac{D^{(1)}/_{LC}}{s^2 - \left(\dfrac{P_o}{CV_c^2}\right)s + \dfrac{1}{LC}} \end{cases} \tag{2.19}$$

Due to CPL, the transfer functions in (2.19) have poles in the right half plane, thus, the system is unstable.

Linear controllers can be designed to stabilize the system around a specific operating point based on a linearized small-signal model, such as that described in (2.19). However, when the operating point (i.e., the input voltage V_i or the load power P_o) significantly changes, the system, which still contains unstable poles, may not be able to be stabilized by using the same linear controller.

2.4 STABILITY ANALYSIS OF MULTI-CONVERTER BUCK-BUCK SYSTEM

2.4.1 Stability of multi-converter buck-buck system

In order to perform a local stability analysis of the system, the system is constituted operating at a certain operating point, see Table 3.1, which presents the parameters value and the operating point to which the system is linearized.

Table 2.1. Values for the physical parameters of the multi-converter buck-buck system.

Par.	Unit	Val. nom.	Description
V_{C1}	V	6,0	Output voltage of source converter (output 1)
P_o	p. u.	0,5	Output power of load converter (output 2)
V_i	V	15,0	DC input voltage
R_{L_1}	Ω	4,0	Load Resistance of source converter
R_{L_2}	Ω	4,0	Load Resistance of load converter
C_1	μF	2000	Capacitor of source converter
C_2	μF	2200	Capacitor of load converter
L_1	mH	2,0	Inductance of source converter
L_2	mH	2,0	Inductance of load converter
r_{L_1}	Ω	0.05	Internal resistance of L_1
r_{L_2}	Ω	0.05	Internal resistance of L_2
D_1	%	42.4	Operational point for duty cycle of output 1
D_2	%	60.0	Operational point for duty cycle of output 2
f_{s_1}	kHz	1.0	Switching frequency of source converter
f_{s_2}	kHz	5.0	Switching frequency of load converter
P_{max}	W	20.0	Maximum power

All the roots of the characteristic polynomial of the system are obtained to verify if all the roots of system are located in the left half of the imaginary plane. In the case that at least one root is in the right half-plane, the entire system is considered unstable [55], [56], [48]. Table 2.2 shows the eigenvalues of the linearized multi-converter buck-buck system.

Table 2.2. Eigenvalues of the linearized multi-converter buck-buck system.

Source Converter
$-62.50 + \mathrm{i}\,496.08$
$-62.50 - \mathrm{i}\,496.08$
Load Converter
-500
-500

All eigenvalues of the system have a negative real part, thus, the system is stable for this point of operation as shown in Table 2.2.

2.4.2 Phase-plane analysis of multi-converter buck-buck system

A system can be analyzed by a phase-plane analysis, solving (plotting) the system differential equations giving an insight about how the system dynamics evolve with time [25], [57], [58]. This technique can be used to study global close-loop behavior of the converter feeding a CPL. The phase-portrait of source converter feeding a CPL is shown in Fig. 2.11 with the physical parameters specified in Table 2.1. The pink line is the load line of the CPL; the blue and red lines represent the trajectory of the state variable $[\, i_{L1} \quad v_{C1} \,]$; the gray arrow indicates the evolving direction of the trajectory. The state plane is divide into two regions by the separatrix (black line): the left region of the separatrix is an unstable region, and the right region of the separatrix is a stable region. Moreover, when the state variable is in the stable region, the trajectory will converge to a limit cycle. On the other hand, when the state variable is in unstable region, any controller cannot guarantee the converter's stability. The phase-portrait of load converter is shown in Fig. 2.12 checking the non-linearity of load converter.

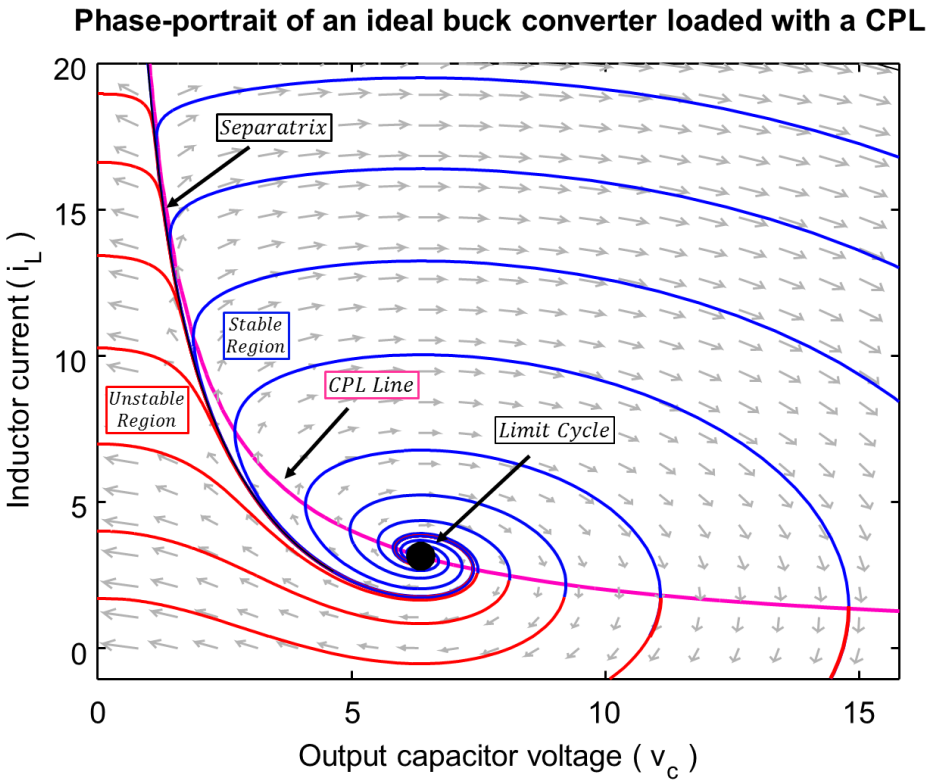

Fig. 2.11. Phase-portrait of source converter loaded with a CPL ($V_i = 15$ V, $D_1 = 0.424$, CPL Power $P_o = 0.5$ p.u., $L = 2$ mH, $C = 2000$ µF).

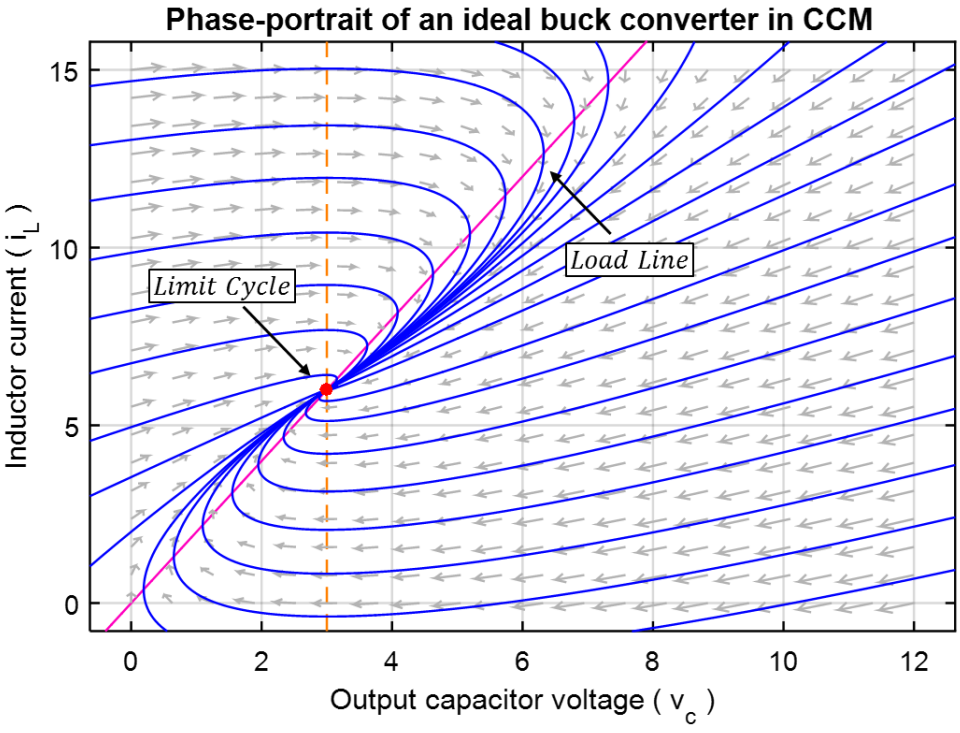

Fig. 2.12. Phase-portrait of load converter (Input DC voltage = 6 V, $D_2 = 0.6$, $P_o = 0.5$ p.u., $L = 2$ mH, $C = 2000$ µF).

2.4 CONCLUSION

In this chapter, the mathematical model that describes the behavior of a multi-converter buck-buck system were present, with its operation and behavior characteristics. The instability problem caused by a CPL in a multi-converter system was described. In addition, the system stability analysis was performed with the operating conditions described in this chapter. The robust controller design methodology will be presented in the next chapter.

CHAPTER 3

ROBUST PARAMETRIC CONTROL: THEORY AND APPLICATION IN THE DESIGN OF ROBUST CONTROLLERS

3.1 INTRODUCCION

Control systems are usually constituted aiming to attend certain close-loop performance desired characteristics. In general, to meet these desired conditions a set of process variables is forced for obtaining the dynamics behavior previously established, thus complying with certain restrictions such as: zero steady-state error, time and frequency requirements, in order to obtain a good dynamic performance.

The controller design is usually based on a linear approximation of nonlinear dynamics systems. However, conventional controllers may experience a sensible performance deterioration under varying operating conditions [14]. In order to assure robustness against varying operating conditions, linear controllers may be designed by using robust control theory. Robust Parametric Control (RPC) Theory, which emerges as a set of modern control techniques, aiming to avoid the negative effects caused by the uncertainties present in the system parameters [45]. The RPC gained greater attention from academia since the 1980s because of Kharitonov's work, who developed the so-called seminal Kharitonov stability Theorem.

In this chapter, some methodologies, for designing of robust parametric controllers, are presented, taking into account a parametric variation in a certain region of uncertainties previously determined by the designer.

3.2 BRIEF REVIEW OF ROBUST CONTROL THEORY

Mathematical models naturally present errors that are neglected, depending on the type of study. An important consideration in model-based control systems is to keep the system stable, subject to parametric variations. However, generally in the classic controller design, models that ignore uncertainties are used [46]. In this way, it is common to use a nominal transfer function for the controller design. Although the controller is developed based on a nominal transfer function, the real system must be stable for all kinds of transfer functions that represent the whole set of uncertainties. Thereby, uncertainty of a system can be classified as unstructured (non-parametric uncertainty) and structured (parametric uncertainty) [43], [45].

Robust parametric control techniques are useful for stability and control analysis of systems subjected to uncertainties in the parameters of the representative models (structured uncertainty).

3.2.1 Robust Stability Analysis

A system with interval parametric uncertainties is generally described by uncertain interval polynomials *B(s)* and *A(s)*, restricted within pre-specified closed real intervals, as shown in (3.1) [45].

$$G(s) = \frac{B(s)}{A(s)} = \frac{\sum_{i=0}^{m}\left[b_i^-,\ b_i^+ \right] s^i}{\sum_{i=0}^{n}\left[a_i^-,\ a_i^+ \right] s^i} \tag{3.1}$$

Many robust stability tests under parametric uncertainty are based on analysis of uncertain characteristic polynomial assumed as an interval polynomial family [45], such as

$$P(s, p) = \sum_{i=0}^{N}\left[p_i^-,\ \ p_i^+ \right] s^i \tag{3.2}$$

where $p = \left(\left[p_0^-,\ \ p_0^+ \right], \left[p_1^-,\ \ p_1^+ \right], ..., \left[p_N^-,\ \ p_N^+ \right] \right)$ is a vector of interval elements.

Polynomial *P(s,p)* is stable if all its roots are contained on the left-hand side of the complex plane s-plane. Then, *P(s,p)* is robustly stable if all its polynomials are stable for a set of operating point different from the nominal operating point within its minimum and maximum limits [49].

Thus, according to [45], two definitions can be defined that characterize the stability concept of the families of polynomials.

Definition 3.1 (Stability): A fixed polynomial *P(s)* is stable if all its roots are strictly located in the left half-plane of the complex plane.

Definition 3.2 (Robust Stability): A certain family of polynomials *P(s,p)* is robustly stable if *P(s,p)* is stable for all $a \in$ R, i.e., all the roots of *P(s,a)* are located strictly in the left half-plane of the complex plane.

3.2.2 Kharitonov Stability Theorem [43]

The Kharitonov Theorem is a test used in robust control theory to evaluate the stability of a dynamic system whose parameters vary within a closed real interval as follows:

$$\delta(s) = \delta_0 + \delta_1 s + \delta_2 s^2 + \delta_3 s^3 + \cdots + \delta_n s^n \tag{3.3}$$

where, the coefficient vector $\overline{\delta} = [\delta_0, \delta_1, \delta_2, \delta_3, \cdots, \delta_n]$ is delimited by:

$$\Delta = \left[\delta_0^-, \delta_0^+\right] \times \left[\delta_1^-, \delta_1^+\right] \times \cdots \times \left[\delta_n^-, \delta_n^+\right] \tag{3.4}$$

where, δ_n^- and δ_n^+ represent the lower and upper limit respectively. Therefore, the Kharitonov polynomials are defined as:

$$
\begin{aligned}
K_1(s) &= \delta_0^- + \delta_1^- s + \delta_2^+ s^2 + \delta_3^+ s^3 + \delta_4^- s^4 + \delta_5^- s^5 + \delta_6^+ s^6 + \cdots \\
K_2(s) &= \delta_0^- + \delta_1^+ s + \delta_2^+ s^2 + \delta_3^- s^3 + \delta_4^- s^4 + \delta_5^+ s^5 + \delta_6^+ s^6 + \cdots \\
K_3(s) &= \delta_0^+ + \delta_1^- s + \delta_2^- s^2 + \delta_3^+ s^3 + \delta_4^+ s^4 + \delta_5^- s^5 + \delta_6^- s^6 + \cdots \\
K_4(s) &= \delta_0^+ + \delta_1^+ s + \delta_2^- s^2 + \delta_3^- s^3 + \delta_4^+ s^4 + \delta_5^+ s^5 + \delta_6^- s^6 + \cdots
\end{aligned}
\tag{3.5}
$$

Theorem 3.1 (Robust Stability): The interval polynomial family delimited by **Δ** is robustly stable if and only if its four Kharitonov polynomials are stable [45], [59], i.e., all roots of the interval polynomial are in the left hand-plane of the complex plane.

3.3 SISO ROBUST CONTROLLER DESIGN VIA INTERVAL POLE-PLACEMENT

To design the controller, a region of uncertainty is previously defined, considering that the uncertainty is contained in the parameter variation of the plant-model. The robust controller design uses two different procedures considering the closed-loop control system in Fig. 3.1. The first is the tool developed in [46], associated with a linear goal programming formulation, which will lead to a set linear inequality constraints. The second procedure is the Chebyshev theorem, developed in [47], which provides a maximum stability region, characterized by a ball of center $\boldsymbol{x_c}$ and radium $\boldsymbol{R}$, whose norm is Euclidean.

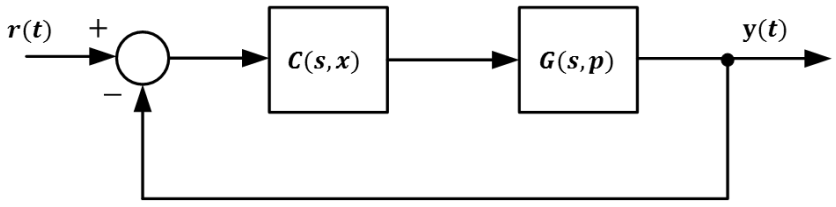

Figure 3.1. Closed-loop system block-diagram.

where *G(s,p)* is the uncertain plant of order *n* and *C(s,x)* is the controller of order *r*, defined in (3.5) and (3.6) respectively. Note that a_i and b_i define the box region of uncertainties denoted by $a_i^- \le a_i \le a_i^+$ and $b_j^- \le b_j \le b_j^+$ for $i = 1,2,\ldots,n;\ j = 1,2,\ldots,m$.

$$
G(s,p) = \frac{n(s)}{d(s)} = \frac{b_1 s^{m-1} + \cdots + b_{m-1} s + b_m}{s^n + a_1 s^{n-1} + \cdots + a_{n-1} s + a_n} \tag{3.5}
$$

$$C(s) = \frac{n_c(s)}{d_c(s)} = \frac{x_0 s^r + x_1 s^{r-1} + \cdots + x_{r-1} s + x_r}{s^r + y_1 s^{r-1} + \cdots + y_{r-1} s + y_r} \tag{3.6}$$

Let ***p*** be the vector of parameters that represent the plant and ***x*** the vector of real parameters representing the controller defined in (3.7) and (3.8) respectively. In addition, p^o represents the nominal value of plant parameters defined in a box region of uncertainties.

$$p := \begin{bmatrix} b_1 & b_2 & \cdots & b_{m-1} & b_n & a_1 & a_2 & \cdots & a_{n-1} & a_n \end{bmatrix} \tag{3.7}$$

$$X := \begin{bmatrix} x_0 & x_1 & \cdots & x_{r-1} & x_r & y_1 & y_2 & \cdots & y_{r-1} & y_r \end{bmatrix} \tag{3.8}$$

According to [60], [61], the solution of the Diophantine equation (3.9) summarizes the pole-placement problem.

$$d(s) = d(s) d_c(s) + n(s) n_c(s) \tag{3.9}$$

where $d(s)$ is the closed-loop characteristic polynomial. Therefore, the parameters of the closed-loop characteristic polynomial are represented as follows:

$$d_i = d_i(x, p) \tag{3.10}$$

Assuming that the desired dynamic of closed-loop system is represented by

$$\Delta_d(s) = s^i + \phi_1 s^{i-1} + \cdots + \phi_{i-1} s + \phi_i \tag{3.11}$$

where ϕ_i represent the parameters of the closed-loop desired polynomial.

Aiming of tuning the controller, the closed-loop parameters obtained are compared with the parameters of the closed-loop desired polynomial, which represent the desired dynamics of the system as a result Eq. (3.12).

$$d_i(x, p^o) = \phi_i, \qquad i = 1, 2, \ldots, l \tag{3.12}$$

This problem can be written in its matrix format, presenting the following relationship:

$$\underbrace{\left[\begin{array}{ccccc|ccccc} [b_1] & 0 & \cdots & 0 & 0 & 1 & 0 & \cdots & 0 & 0 \\ [b_2] & [b_1] & \ddots & \vdots & 0 & [a_1] & 1 & \ddots & \vdots & 0 \\ \vdots & [b_2] & \ddots & 0 & \vdots & \vdots & [a_1] & \ddots & 0 & \vdots \\ [b_{m-1}] & \vdots & \ddots & [b_1] & 0 & [a_{n-1}] & \vdots & \ddots & 1 & 0 \\ [b_m] & [b_{m-1}] & \ddots & [b_2] & [b_1] & [a_n] & [a_{n-1}] & \ddots & [a_1] & 1 \\ 0 & [b_m] & \ddots & \vdots & [b_2] & 0 & [a_n] & \ddots & \vdots & [a_1] \\ \vdots & 0 & \ddots & [b_{m-1}] & \vdots & \vdots & 0 & \ddots & [a_{n-1}] & \vdots \\ 0 & \vdots & \ddots & [b_m] & [b_{m-1}] & 0 & \vdots & \ddots & [a_n] & [a_{n-1}] \\ 0 & 0 & \cdots & 0 & [b_m] & 0 & 0 & \cdots & 0 & [a_n] \end{array}\right]}_{A} \underbrace{\left[\begin{array}{c} x_0 \\ x_1 \\ \vdots \\ x_{r-1} \\ x_r \\ - \\ y_0 \\ y_1 \\ \vdots \\ y_{r-1} \\ y_r \end{array}\right]}_{X} = \underbrace{\left[\begin{array}{c} [\phi_1]-[a_1] \\ [\phi_2]-[a_2] \\ \vdots \\ [\phi_n]-[a_n] \\ [\phi_{n+1}] \\ \vdots \\ [\phi_m] \end{array}\right]}_{B} \tag{3.13}$$

When the system is subject to parametric uncertainties, the controller performance may deteriorate. Therefore, the controller must guarantee robust performance within an acceptable region of closed-loop parameters variation, so that the closed-loop poles are located in a certain region. Thereby, a desired region is defined as follows:

$$\Phi := \left\{ \phi_i^- \le \phi_i \le \phi_i^+ \right\} \tag{3.14}$$

Therefore, according to [49], replacing the parameters of equation (3.14) in equation (3.12), it is possible to formulate a linear inequalities set, which restricted the controller and desired polynomial coefficients in the predefined intervals, as shown in Eq. (3.15). Thus, the closed-loop system has its poles within the roots space of interval-desired polynomial, ensuring the robust stability [60].

$$\phi_i^- \le d_i(x, p) \le \phi_i^+, \qquad i = 1, 2, \ldots, l \tag{3.15}$$

The condition in Eq. (3.15) can be illustrated by Eq. (3.16), assuring stability and performance requirements [60].

$$\Re\big(d(s)\big) \subseteq \Re\big(\Delta_d(s)\big) \tag{3.16}$$

where $\Re\left(d(s)\right)$ denotes the roots space or polynomial poles of $d(s)$ and $\Re\left(\Delta_d(s)\right)$ denotes the roots space of desired polynomial family $\Delta_d(s)$.

The solution of this problem can be idealized, as a solution to a linear programming problem, therefore different techniques can be used to solve it. However, its standard solution is sometimes efficient and fast, so that this problem can be rewritten as a problem of local minimization, subject to restrictions, according to relations defined in [46], [43], [45] [39], [40], and [41].

3.3.1 Linear Programing based on Kharitonov's Rectangle

The coefficients of vector $\boldsymbol{X}$ can be calculated by using the linear programming technique as shown below [49],

$$\begin{aligned} &X = \arg\left(\min \ \ f(X)\right) \\ &s.t. \begin{bmatrix} A_{upper} \\ -A_{lower} \end{bmatrix} X \le \begin{bmatrix} B(\phi^+) \\ -B(\phi^-) \end{bmatrix} \end{aligned} \tag{3.17}$$

where,

$$A_{upper} = \left[\begin{array}{ccccc|ccccc} b_1^+ & 0 & \cdots & 0 & 0 & 1 & 0 & \cdots & 0 & 0 \\ b_2^+ & b_1^+ & \ddots & \vdots & 0 & a_1^+ & 1 & \ddots & \vdots & 0 \\ \vdots & b_2^+ & \ddots & 0 & \vdots & \vdots & a_1^+ & \ddots & 0 & \vdots \\ b_{m-1}^+ & \vdots & \ddots & b_1^+ & 0 & a_{n-1}^+ & \vdots & \ddots & 1 & 0 \\ b_m^+ & b_{m-1}^+ & \ddots & b_2^+ & b_1^+ & a_n^+ & a_{n-1}^+ & \ddots & a_1^+ & 1 \\ 0 & b_m^+ & \ddots & \vdots & b_2^+ & 0 & a_n^+ & \ddots & \vdots & a_1^+ \\ \vdots & 0 & \ddots & b_{m-1}^+ & \vdots & \vdots & 0 & \ddots & a_{n-1}^+ & \vdots \\ 0 & \vdots & \ddots & b_m^+ & b_{m-1}^+ & 0 & \vdots & \ddots & a_n^+ & a_{n-1}^+ \\ 0 & 0 & \cdots & 0 & b_m^+ & 0 & 0 & \cdots & 0 & a_n^+ \end{array}\right] \tag{3.18}$$

$$A_{lower} = \begin{bmatrix} \bar{b_1} & 0 & \cdots & 0 & 0 & | & 1 & 0 & \cdots & 0 & 0 \\ \bar{b_2} & \bar{b_1} & \ddots & \vdots & 0 & | & \bar{a_1} & 1 & \ddots & \vdots & 0 \\ \vdots & \bar{b_2} & \ddots & 0 & \vdots & | & \vdots & \bar{a_1} & \ddots & 0 & \vdots \\ \bar{b_{m-1}} & \vdots & \ddots & \bar{b_1} & 0 & | & \bar{a_{n-1}} & \vdots & \ddots & 1 & 0 \\ \bar{b_m} & \bar{b_{m-1}} & \ddots & \bar{b_2} & \bar{b_1} & | & \bar{a_n} & \bar{a_{n-1}} & \ddots & \bar{a_1} & 1 \\ 0 & \bar{b_m} & \ddots & \vdots & \bar{b_2} & | & 0 & \bar{a_n} & \ddots & \vdots & \bar{a_1} \\ \vdots & 0 & \ddots & \bar{b_{m-1}} & \vdots & | & \vdots & 0 & \ddots & \bar{a_{n-1}} & \vdots \\ 0 & \vdots & \ddots & \bar{b_m} & \bar{b_{m-1}} & | & 0 & \vdots & \ddots & \bar{a_n} & \bar{a_{n-1}} \\ 0 & 0 & \cdots & 0 & \bar{b_m} & | & 0 & 0 & \cdots & 0 & \bar{a_n} \end{bmatrix} \tag{3.19}$$

$$B(\phi^{+}) = \begin{bmatrix} \phi_1^{+} - \bar{a_1} \\ \phi_2^{+} - \bar{a_2} \\ \vdots \\ \phi_n^{+} - \bar{a_n} \\ \phi_{n+1}^{+} \\ \vdots \\ \phi_m^{+} \end{bmatrix} \qquad B(\phi^{-}) = \begin{bmatrix} \phi_1^{-} - a_1^{+} \\ \phi_2^{-} - a_2^{+} \\ \vdots \\ \phi_n^{-} - a_n^{+} \\ \phi_{n+1}^{-} \\ \vdots \\ \phi_m^{-} \end{bmatrix} \tag{3.20}$$

3.3.2 Linear Programing based on Chebyshev Theorem

The Chebyshev Theorem demonstrate that it is possible to find the largest ball ***B*** of center $\boldsymbol{x_c}$ and maximum radius ***R***, whose norm is Euclidean, which is contained in the polytope ***P***, described by the set of linear inequalities constraints. The ball center $\boldsymbol{x_c}$ is called Chebyshev Center, as shown in Fig. 3.2 [47].

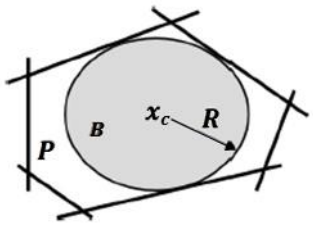

Figure 3.2. Largest ball B inscribed in P.

when the set ***P*** is convex, the computing of $\boldsymbol{x_c}$ become a convex optimization problem. More specifically, suppose $P \subseteq R^n$ is defined by a set of convex inequalities, i.e. $P = \{a_i x \le b_i,\ i = 0,1,\ldots,m\}$. If $R \ge 0$, it can be found $\boldsymbol{x_c}$ by solving the Linear Programming according to following relations:

$$X' = \arg\left(\min \quad f(X')\right)$$
$$s.t. \begin{bmatrix} A'_{upper} \\ -A'_{lower} \end{bmatrix} X' \leq \begin{bmatrix} B(\phi^{+}) \\ -B(\phi^{-}) \\ 0 \end{bmatrix} \tag{3.21}$$

where,

$$X' = \begin{bmatrix} X \\ R \end{bmatrix} \tag{3.22}$$

$$A' = \begin{bmatrix} A_i & \|a_i\| \\ -A_i & \|a_i\| \\ 0_{1\times i} & -1 \end{bmatrix}, \|a_i\| \text{ is the norm of coefficients of } A_i \tag{3.23}$$

$$A'_{upper} = \begin{bmatrix} A_{upper} & \|a_{upper}\| \\ -A_{upper} & \|a_{upper}\| \\ 0_{1\times n} & -1 \end{bmatrix} \tag{3.24}$$

$$A'_{lower} = \begin{bmatrix} A_{lower} & \|a_{lower}\| \\ -A_{lower} & \|a_{lower}\| \\ 0_{1\times n} & -1 \end{bmatrix} \tag{3.25}$$

3.3.3 Summary of the methodology

Fig. 3.3 illustrates a simplified flowchart of the methodology for designing the robust controller based on intervals pole-placement. The adopted strategy is an adaptation of the algorithm proposed in [39]. The process starts in step 1, by defining the nominal plant with its operating conditions; in step 2, the box region of uncertainties is built based on a previously specified uncertainty range delimited by the designer. The closed-loop polynomial is obtained by using the controller parameter and the nominal model selected in step 1, then by replacing the nominal and interval values, defined in step 2, the interval closed-loop polynomial is calculated (step 3). In step 4, the desired performance polynomial must be chosen. The optimization problem is selected in step 5 and in step 6 is solved. In step 6(A), the cost function

is defined as the sum of controller gains and the parameter vector X contains the controller gains. In step 6(B), the cost function is defined as the sum of controller gains with the radio R and the parameter vector X contains the controller gains and the radio of Chebyshev sphere. The feasible solution X^* (obtained in step 5) is used to set the control structure (step 7).

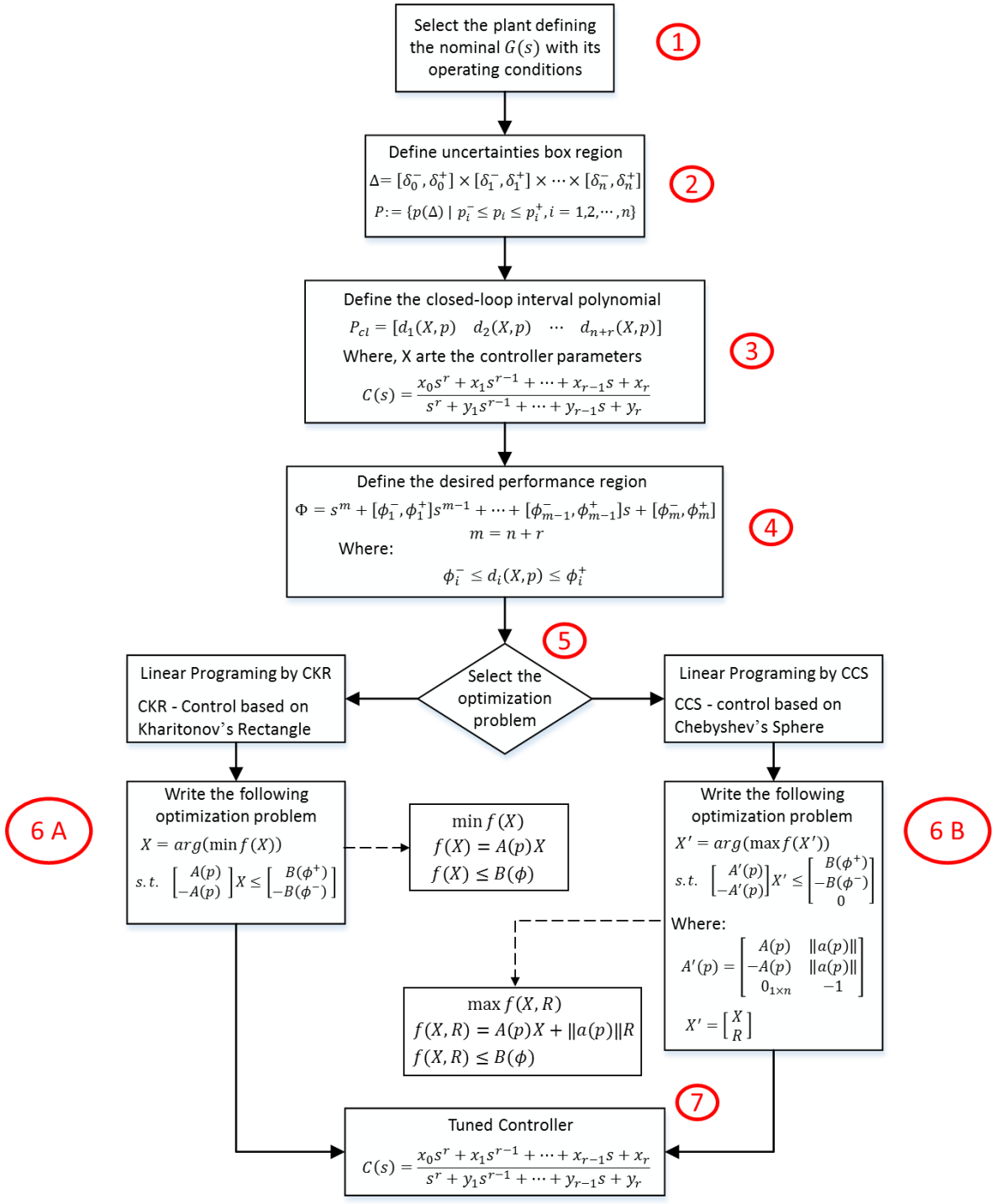

Figure 3.3. Flowchart of methodology for designing of robust controllers.

3.4 CONCLUSION OF THE CHAPTER

In this chapter, some different design methodologies of robust controllers were presented. Brief theoretical and mathematical concepts of robust control theory were also introduced. The next chapter will present the methodology used for the development of this work, as well as the development of the simulation and experimental environment for the realization of the study.

CHAPTER 4

DESCRIPTION OF TEST ENVIRONMENTS

4.1 INTRODUCCION

In this chapter, the methodology adopted to carry out this study is discussed, as well as the tests developed in the system in analysis, a multi-converter buck-buck system. It also presents the computational environment and the experimental environment of the developed system.

4.2 CONTROLLER DESIGN BY CLASSICAL POLE-PLACEMENT

To tune the controller by Classical Pole-Placement (CPP) method, the performance specifications related to the settling time (T_s) and maximum overshoot (O_s) were used as a restriction for the design of the controller. Table 4.1 presents the performance specifications values for the development of the control design for Voltage Mode Control (VMC) of source converter.

Table 4.1. Performance specifications for the controller design of source converter.

Design specifications	***Symbol***	***Unit***	***Design restriction***
Settling Time	T_s	ms	≤ 100
Overshoot	O_s	%	≤ 5

Table 4.2 presents the performance specifications values for the development of the control design for Power Mode Control (PMC) of load converter. Table 4.3 presents the controller parameters values based on CPP method.

Table 4.2. Performance specifications for the controller design of load converter.

Design specifications	*Symbol*	*Unit*	*Design restriction*
Settling Time	T_s	ms	≤ 50
Overshoot	O_s	%	≤ 5

The desired characteristic polynomial is calculated by the design specifications and the system parameters values used in the desired operation point (see Table 2.1), locating an auxiliary pole where this pole is a non-dominant pole of system, therefore their characteristic do not influence in the system behavior, as presented in Equation 4.1 and 4.2. Equation 4.1 is for VMC of source converter, and Equation 4.2 is for PMC of load converter. The location of these no dominant poles is at the discretion of designer.

$$\begin{aligned} P_d(s) &= \left(s + a_{Aux}\right)\left(s^2 + 2\xi_d \omega_{n_d} s + \omega_{n_d}^2\right) \\ P_d(s) &= \left(s + 40\right)\left(s^2 + 2(0.1519)(503.28)s + 503.28^2\right) \end{aligned} \tag{4.1}$$

$$\begin{aligned} P_d(s) &= \left(s + a_{Aux}\right)\left(s^2 + 2\xi_d \omega_{n_d} s + \omega_{n_d}^2\right) \\ P_d(s) &= \left(s + 40\right)\left(s^2 + 2(0.8)(500)s + 500^2\right) \end{aligned} \tag{4.2}$$

4.3 ROBUST CONTROLLER DESIGN BY INTERVAL POLE-PLACEMENT

To tune the controller by interval pole-placement, it is necessary to define the uncertainties region in which the plant parameters will be subjected. Table 4.3 presents the uncertain parameters value adopted for the development of the robust controller design.

Table 4.3. Values for the physical parameters of the multi-converter buck-buck system with its parametric uncertainties for the experimental tests.

Par.	Unit	Var. (%)	Val. nom.	Val. Max.	Val. Min.	Description
V_{C1}	V	–	8,0	–	–	Output voltage of source converter
P_o	p. u.	0,4	–	–	–	Output power of load converter
V_i	V	15	15,0	17,25	12,75	DC input voltage
R_{L_1}	Ω	50	4,0	6,0	2,0	Load Resistance of source converter
R_{L_2}	Ω	–	4,0			Load Resistance of load converter
C_1	μF	–	2000	–	–	Capacitor of source converter
C_2	μF	–	2200	–	–	Capacitor of load converter
L_1	mH	–	2,0	–	–	Inductance of source converter
L_2	mH	–	2,0	–	–	Inductance of load converter
r_{L_1}	Ω	15	0.05	–	0,0425	Internal resistance of L_1
r_{L_2}	Ω	–	0.05	–	0,0575	Internal resistance of L_2
D_1	%	–	74.4	–	–	Operational point for duty cycle of
D_2	%	–	63.2	–	–	Operational point for duty cycle of
f_{s_1}	kHz	–	1.0	–	–	Switching frequency of source
f_{s_2}	kHz	–	5.0	–	–	Switching frequency of load converter
P_{max}	W	–	20.0	–	–	Maximum power

Thereby, the gains of the robust controller can be tuned, as presented by the methodology described in chapter 3, Control based on Kharitonov's Rectangle (CKR) and Control based on Chebyshev's Sphere (CCS). Table 4.4 presents the gains value of the controllers designed for the three methodologies evaluated by this study using the continuous PID controller structure.

$$C_{PID}(s) = \frac{u(s)}{e(s)} = \frac{k_d s^2 + k_p s + k_i}{s} \tag{4.3}$$

Table 4.4. Parameters value for the designed controllers.

	VMC $C_1(s)$			PMC $C_2(s)$
	CPP	CKR	CCS	CPP
k_d	1.2023e^{-5}	1.0588e^{-5}	1.0176e^{-5}	2.49916e^{-5}
k_p	-0.009997	0.010814	0.011815	-0.025413
k_i	2.4169	2.6783	2.9109	51.6969

In order to develop the digital application of the controllers designed by the methods addressed in this study, applied in the multi-converter system, it is necessary to obtain the discrete equivalent of the controllers, to then implement them in computerized hardware, by equation to differences. Thereby, an indirect method of controller design is used, in order to obtain the controller in the discrete domain through an approximation.

In order to obtain the discrete equivalent of the designed controllers, the ZOH method [48], [55], [56], was used to perform the discrete approximation, using as a selection criterion of sampling frequency between 2 to 10 greater than the frequency band of system, the period was selected sampling rate of 1 *ms*.

Equation 4.4 presents the generic form for obtaining the discrete gains of the digital PID controller. Table 4.5 presents the discrete controller gains value for each methodology discussed in this study, based on the indirect method of controller design [48], [55], [56].

$$C_{PID}(z) = \frac{r_0 z^2 + r_1 z + r_2}{z^2 - z} \tag{4.3}$$

Table 4.5. Discrete parameters value for the designed controllers.

	VMC $C_1(z)$			PMC $C_2(z)$
	CPP	CKR	CCS	CPP
r_0	0.01135786	0.02408077	0.02490183	0.27619610
r_1	−0.01876711	−0.03199080	−0.03216709	−0.47441176
r_2	0.01002328	0.01058834	0.01017621	0.24991257

4.4 PRESENTATION AND DESCRIPTION OF THE SIMULATION ENVIRONMENT OF THE MULTI-CONVERTER BUCK-BUCK SYSTEM

For the development of the multi-converter buck-buck system, two SISO controllers are used to regulate system outputs, the first one to control the output voltage of source converter and the second one to control the output power of load converter. Fig. 4.1 presents a control-generalized block-diagram applying to multi-converter buck-buck system, using filters in the outputs of system to avoid that ripples of the outputs interfere in the performance of the designed controller. These filters must be designed so that they do not affect the system dynamics. Fig. 4.2 presents the electric circuit of the multi-converter buck-buck, as well as the application of robust control to system.

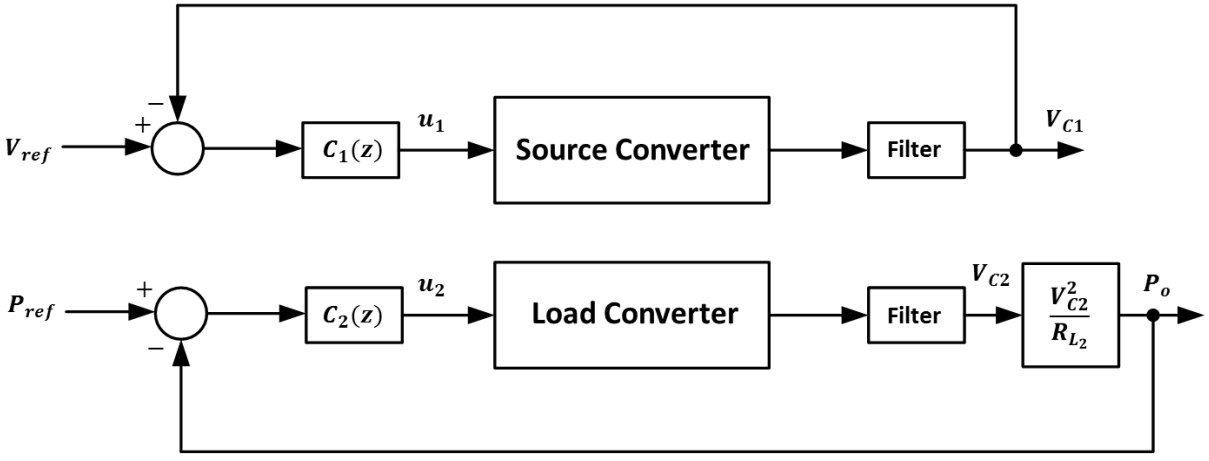

Figure 4.1. Control-generalized block-diagram applying to multi-converter buck-buck system

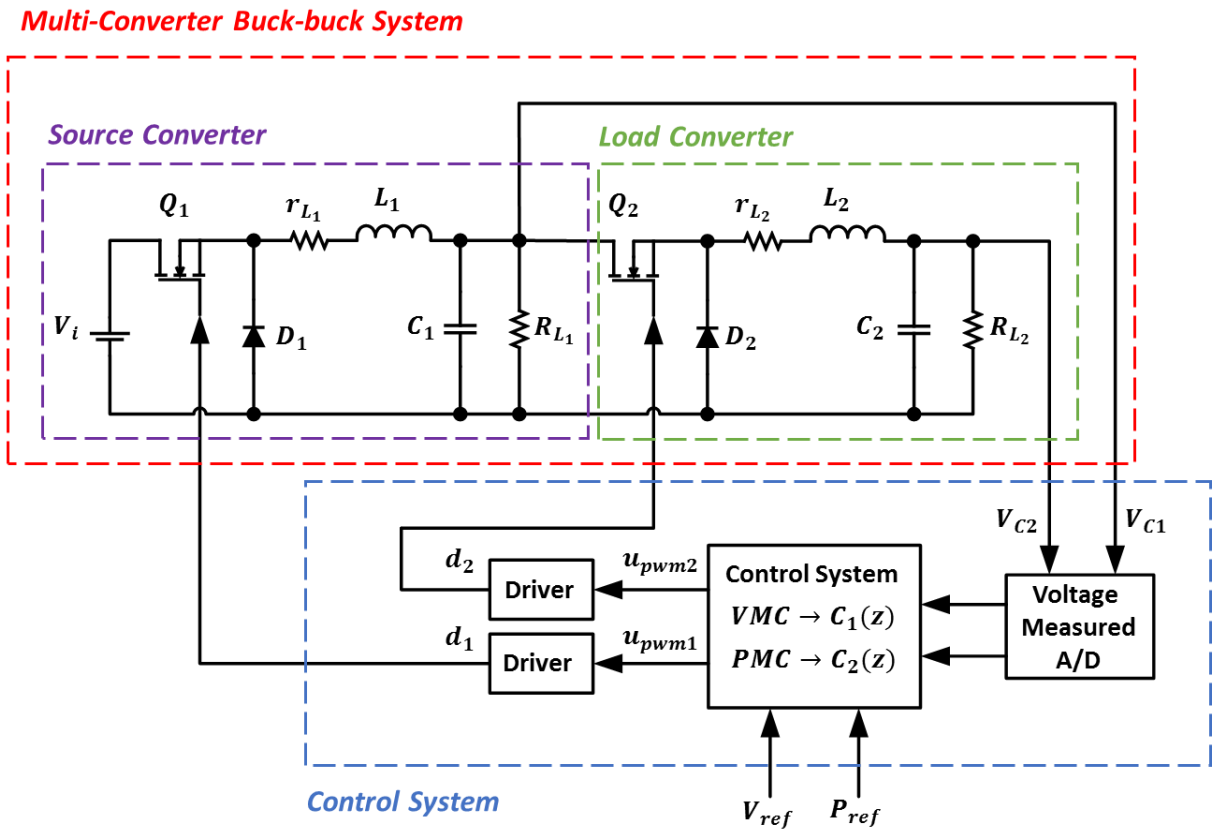

Figure 4.2. The electric circuit of the multi-converter buck-buck system.

4.4.1 Simulation environment of the multi-converter buck-buck system

Simulation is carried out in Matlab/Simulink computational environment in order to simulate the multi-converter buck-buck system with its non-linear characteristics. The controllers design is performed for the system linearized around a certain operating point, and the discrete equivalent of the controllers is used for all the tests in simulation environment. However all experiments in computational environment are performed with simulations of the non-linear model of the multi-converter buck-buck system. Fig. 4.3 (A) presents the block-diagram developed in Matlab/Simulink for the non-linear simulation of the multi-converter buck-buck system. The so-called powersim toolbox is used, which allows the use of electrical and electronic components for system development. Fig. 5.3 (B) and (C), respectively, present the control subsystems 1 and 2, thereby, to apply the control into static key, two systems are developed to generate saw-tooth waves with a frequency of 1 and 5 kHz, respectively. Then a

comparator is used to provide PWM (Pulse With Modulation) regulation, which are derived from the control signals obtained at the outputs of the designed controllers.

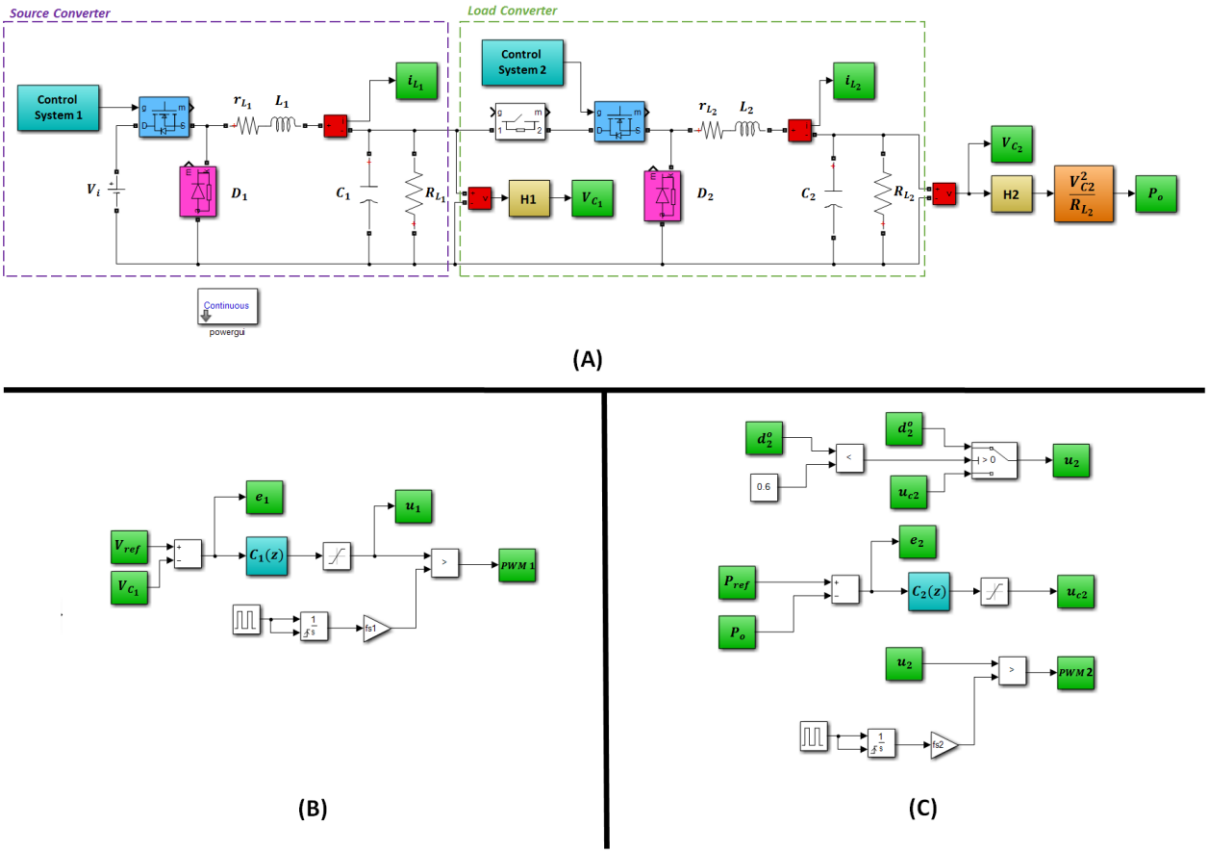

Figure 4.3. (A) Electric circuit of the multi-converter buck-buck system by Matlab/Simulink. (B) Control subsystem 1. (C) Control subsystem 2.

4.4.2 Experimental environment of the multi-converter buck-buck system

For the development of the experimental environment, subsystems are constituted for performing the tests proposed by this work. Fig. 4.4 presents a generic diagram of the subsystems developed to aid in the development of the tests.

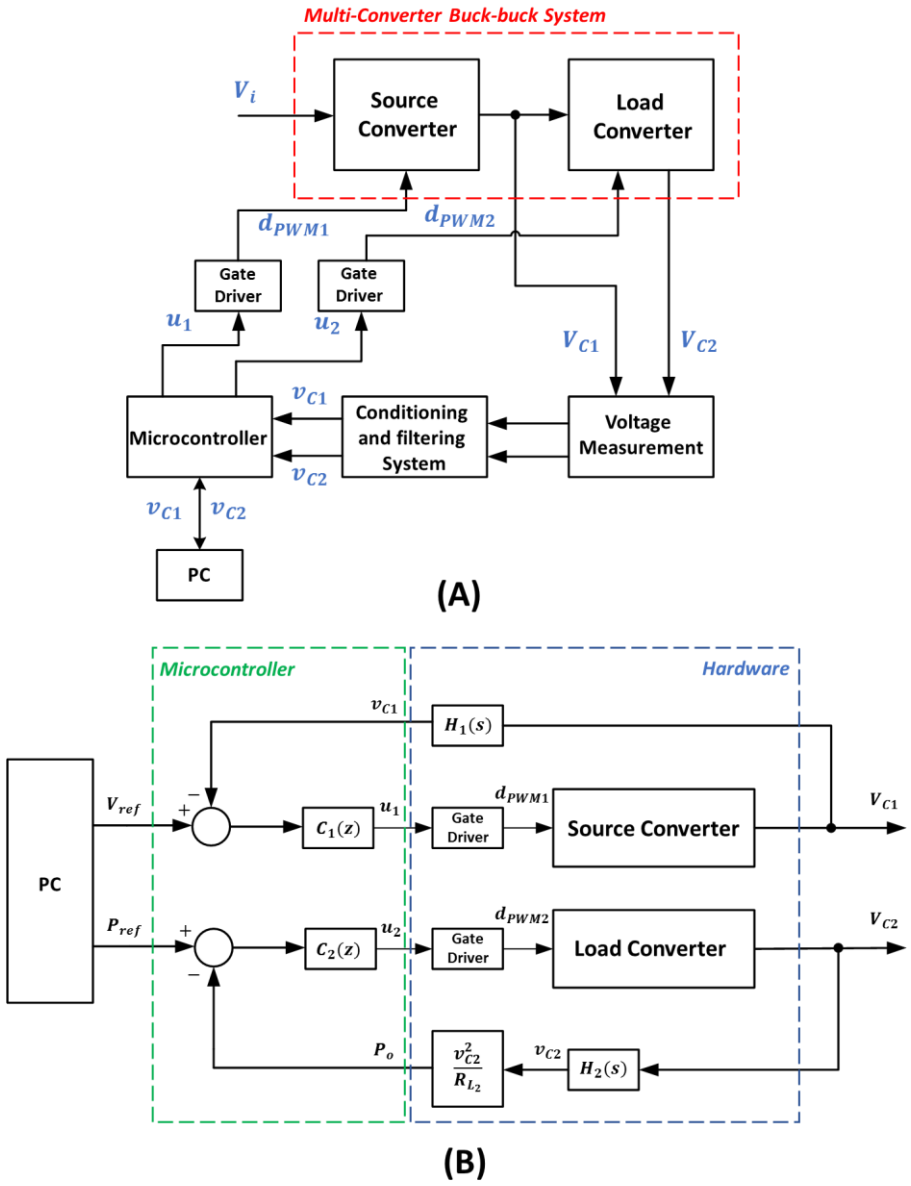

Figure 4.4. (A) Generic diagram of the subsystems developed. (B) Block diagram of the developed hardware system and actuation of the system control signal.

Where, $H_1(s)$ and $H_2(s)$ represent the filters designed to minimize the ripples of outputs 1 and 2 of system, respectively. According to the development proposal of the systems and subsystems to be used for performance of the tests, the physical system is developed with its subsystems presented in Fig. 4.4 (A) and (B). Fig. 4.5 shows the system developed for the experimental study.

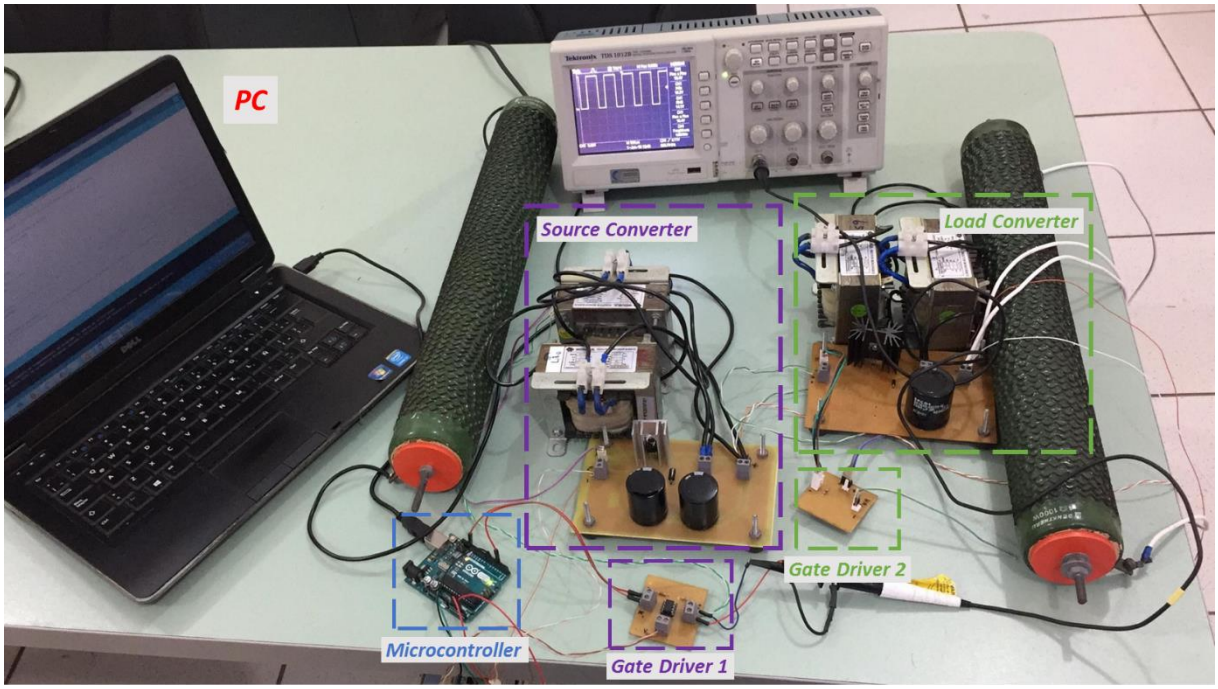

Figure 4.5. Multi-converter buck-buck system.

4.5 DESCRIPTION OF EXPERIMENTS

To carry out an adequate evaluation of the control strategies applying to the multi-converter buck-buck system developed in an experimental and a simulated environment, a sequence of experiments is carried out when source converter is feeding a CPL for different operating points of the power control. The simulated and experimental tests are performed according to the operating condition described in Table 4.3. The parameters of source converter are not changed, only the controller gains. For power control of load converter, the controller parameter are calculated using the performance specifications in Table 4.2 and the operating condition in Table 4.3. Table 4.4 presents the gains value of the controllers designed for the experimental using the continuous PID controller structure.

4.5.1 Evaluation of voltage mode control of source converter.

This experiment aims to perform a behavior evaluation of the control strategies, when source converter does not feed load converter, verifying that the pre-established performance conditions, for controller design, are fulfilled. The simulated and experimental tests are evaluated as follows. The source converter is set to its initial operating condition, as mentioned in Table 4.3, until the steady state is achieved operating in closed-loop being controlled by designed controllers. Thereafter, the system is subjected to a reference voltage variation from 8 V to 9 V, then form 9 V to 8 V and finally, from 8 V to 7 V.

4.5.2 Evaluation of power mode control of load converter.

This experiment aims to perform a behavior evaluation of the control strategy, when load converter is not powered by source converter but is powered by a fixed voltage source of 6 V and 8 V for simulated and experimental test, respectively, according to its operating point defined in Table 4.3. The simulated and experimental tests are evaluated as follows. First, the load converter operates in open-loop until the operation point of duty cycle is achieved. Then, the load converter operates in closed-loop with the designed controller. Finally, after the steady state is achieved, the system is subjected to a reference power variation from 0.3 p.u. to 0.4 p.u., then from 0.4 p.u. to 0.3 p.u. verifying that the pre-established performance conditions, for controller design, are fulfilled.

4.5.3 Performance evaluation of source converter feeding a CPL

This experiment aims to perform a behavior evaluation of the control strategies, when source converter is feeding load converter, which operates as a CPL. The simulated and experimental tests are evaluated as follows. First, The source converter is set to its initial operating condition, as mentioned in Table 4.6, until the steady state is achieved operating in closed-loop being controlled by designed controllers. Then, source converter starts feeding load

converter, which starts to operate in open-loop until the operation point of duty cycle is achieved. After that, load converter operates in closed-loop with the designed controller. Finally, after the steady state is achieved, the multi-converter is subjected to a reference power variation in an operating range of ± 0.5 p.u., verifying that the pre-established performance conditions are fulfilled.

4.6 CONCLUSION OF THE CHAPTER

In this chapter the simulation and experimental environments developed for the tests proposed in this work were presented and described. All experiments to be carried out for this research were described. The next chapter, the results obtained by this study will be analyzed.

CHAPTER 5
RESULTS ANALYSIS

5.1 INTRODUCCION

This chapter presents and discusses the results obtained by simulation using the Matlab/Simulink computational environment and via experimental tests carried out on the developed platform of the multi-converter buck-buck system. The tests developed are described in chapter 4 and the results are presented in this chapter. Four tests are performed: i) evaluation of voltage mode control of source converter; ii) Evaluation of power mode control of load converter; iii) Performance evaluation of source converter feeding a CPL under positive power variation; iv) Performance evaluation of source converter feeding a CPL under negative power variation.

5.2 EVALUATION OF VOLTAGE MODE CONTROL OF SOURCE CONVERTER

Aiming to develop a performance evaluation of the control methodologies evaluated in this work, when the source converter is not feeding the load converter. A variation in reference voltage is performed in order to verify that the pre-established performance conditions of closed-loop system are fulfilled.

5.2.1 Simulation environment

In the previous chapter, the description is presented for performance of this experiment, thus, the non-linear system developed in Matlab/Simulink is used to evaluate the performance of control strategies applied to source converter in order to verify the robustness of the control strategies under variation of the reference voltage in a variation range of ± 1 V of its operating point. Fig. 5.1 shows the result obtained from the non-linear simulation of the source converter

controlled by a PID controller, when the system is subjected to a reference voltage variation from 8 V to 9 V, then form 9 V to 8 V and finally, from 8 V to 7 V.

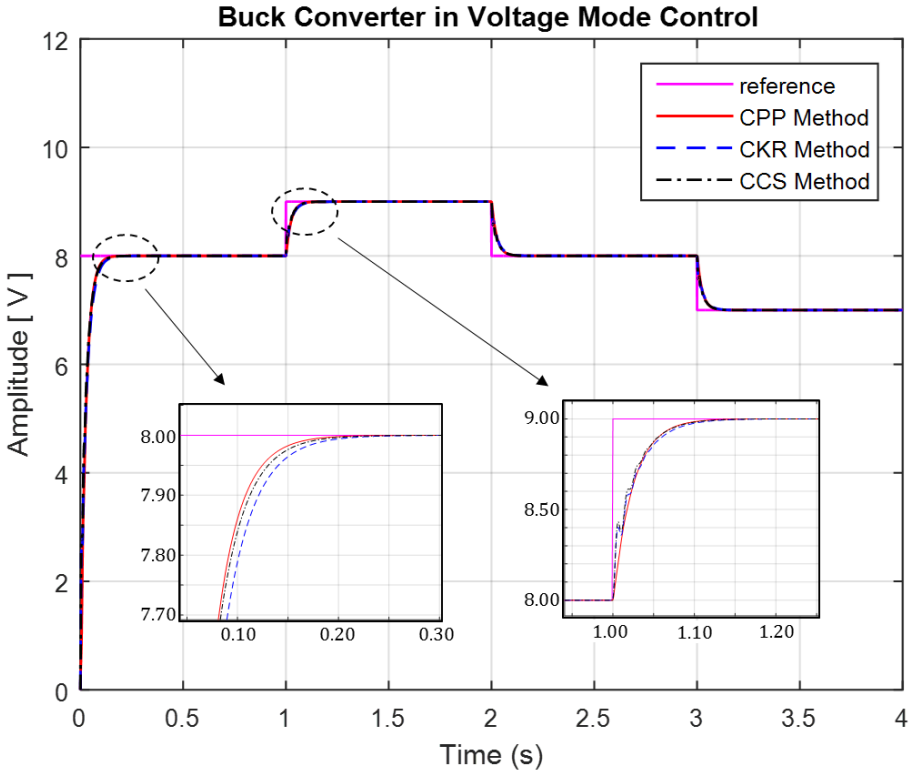

Figure 5.1. Source Converter operating in closed-loop with a PID controller structure.

Fig. 5.1 shows that the three controllers met the performance specifications in closed loop, tracking the reference for the entire range of its operating point variation. However, the controller tuned by CCS method obtained a better ISE performance index than those obtained by CKR and CPP methods as shown in Fig. 5.2. Fig. 5.3 shows the control effort by using a PID control structure. Note that all methods obtained a similar performance, so the control effort will be similar as shown in figure 5.4.

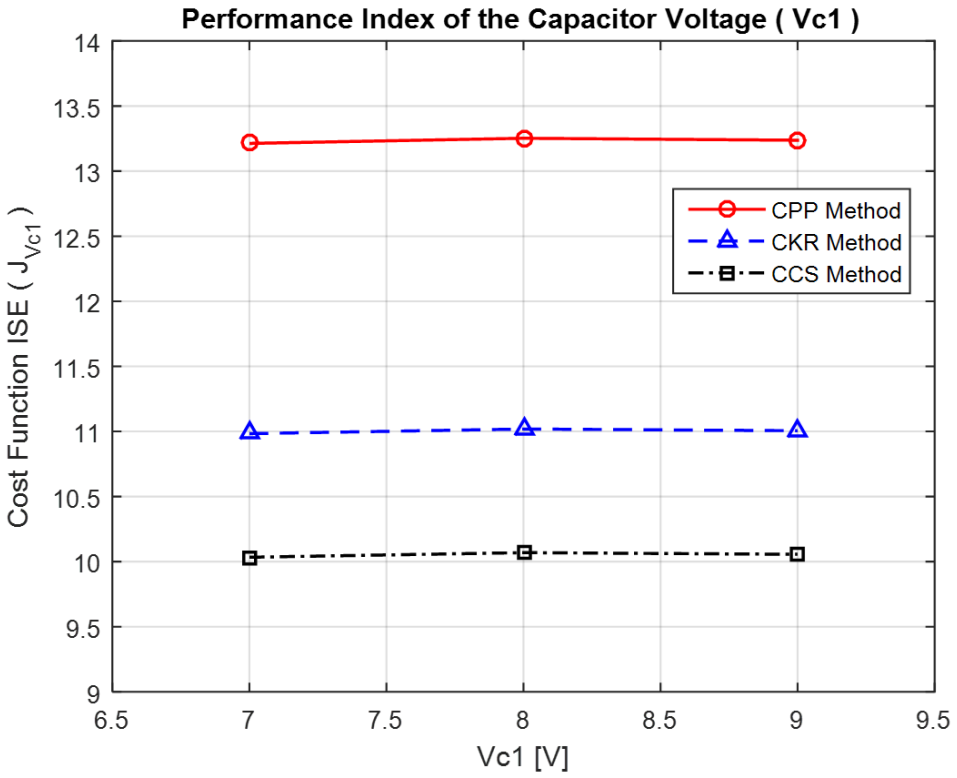

Figure 5.2. The cost function ISE of the simulated system when the source converter is subjected to a reference voltage variation using a PID control structure.

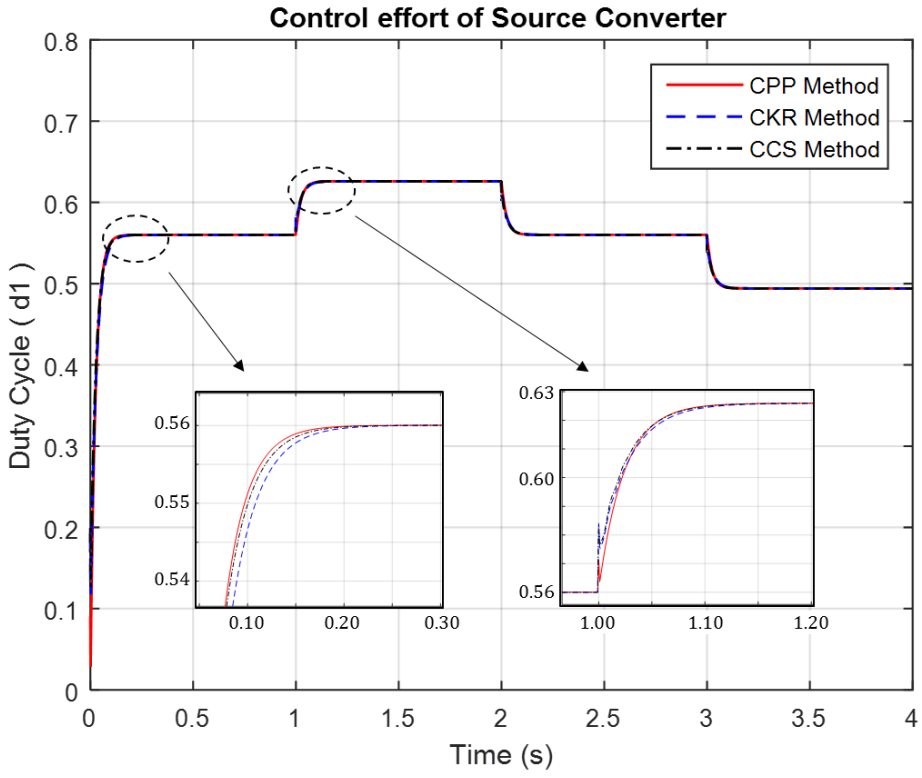

Figure 5.3. The control effort test, when the source converter is subjected to a reference voltage variation using a PID control structure.

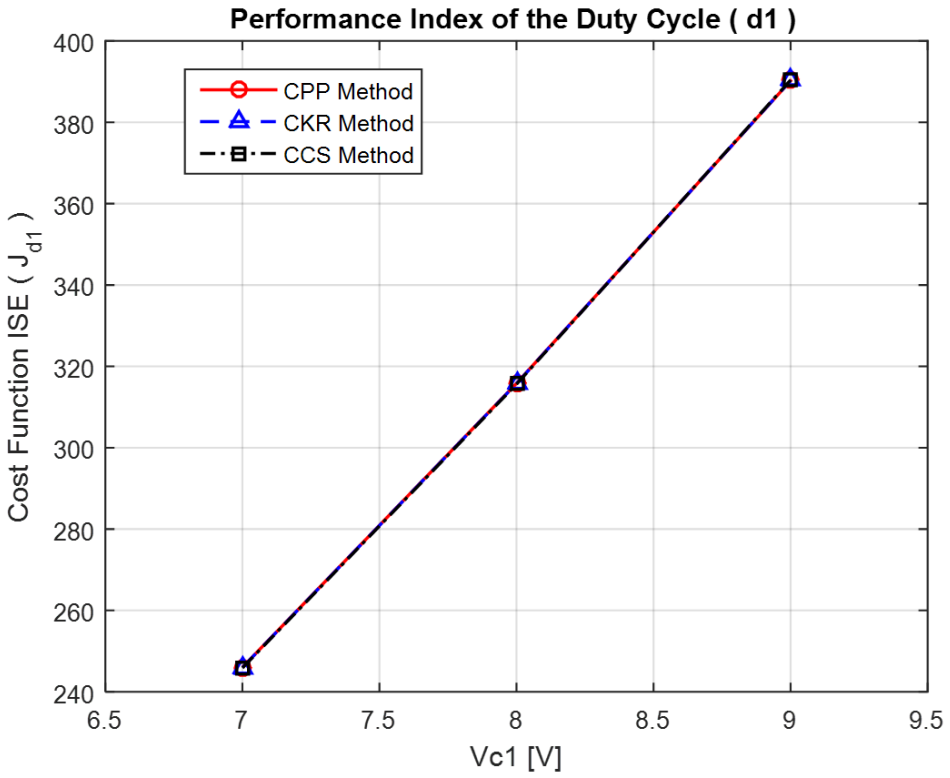

Figure 5.4. The cost function ISE of control effort of the simulated system when the source converter is subjected to a reference voltage variation using a PID control structure.

5.2.2 Experimental environment

Tests in the experimental environment are carried out in the same way as in the simulation environment. Fig. 5.5 shows the experimental evaluation performed in the source converter, using a PID control structure, when the system is subjected to a reference voltage variation from 8 V to 9 V, then from 9 V to 8 V and finally, from 8 V to 7 V. Note that all methods have succeeded in tracking reference for the entire range of variation of its operating point. However, the controller tuned by CCS method obtained a better ISE performance index than those obtained by CKR and CPP methods as shown in Fig. 5.6. Fig. 5.7 shows the control effort by using a PID control structure. Fig. 5.8 shows the ISE performance index of the control effort.

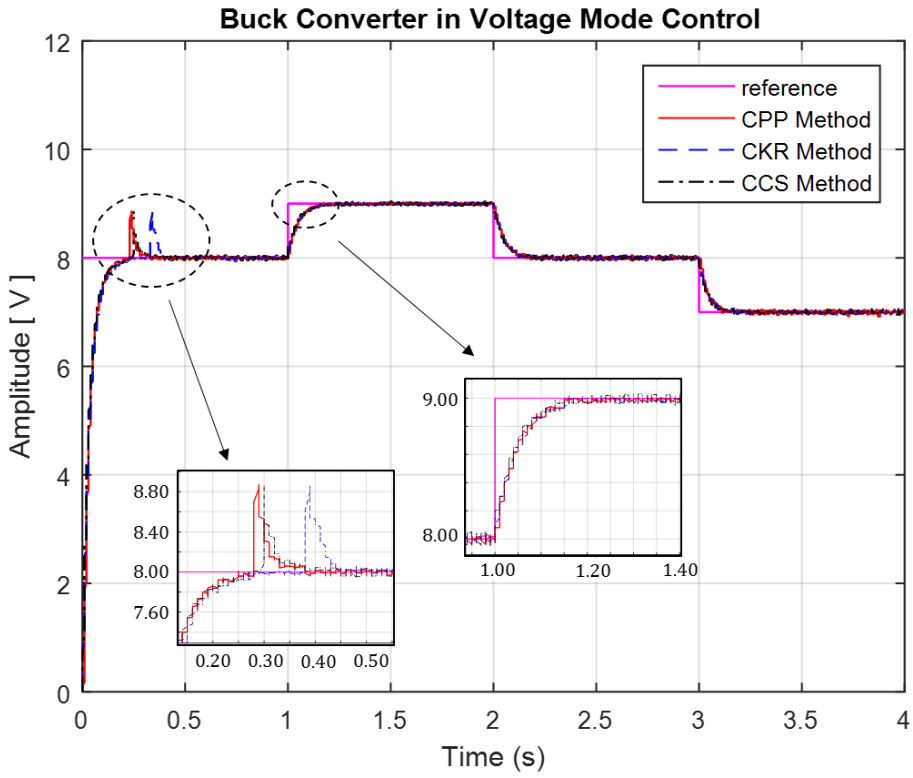

Figure 5.5. Experimental test of the source converter using a PID control structure when the system is subjected to a reference voltage variation.

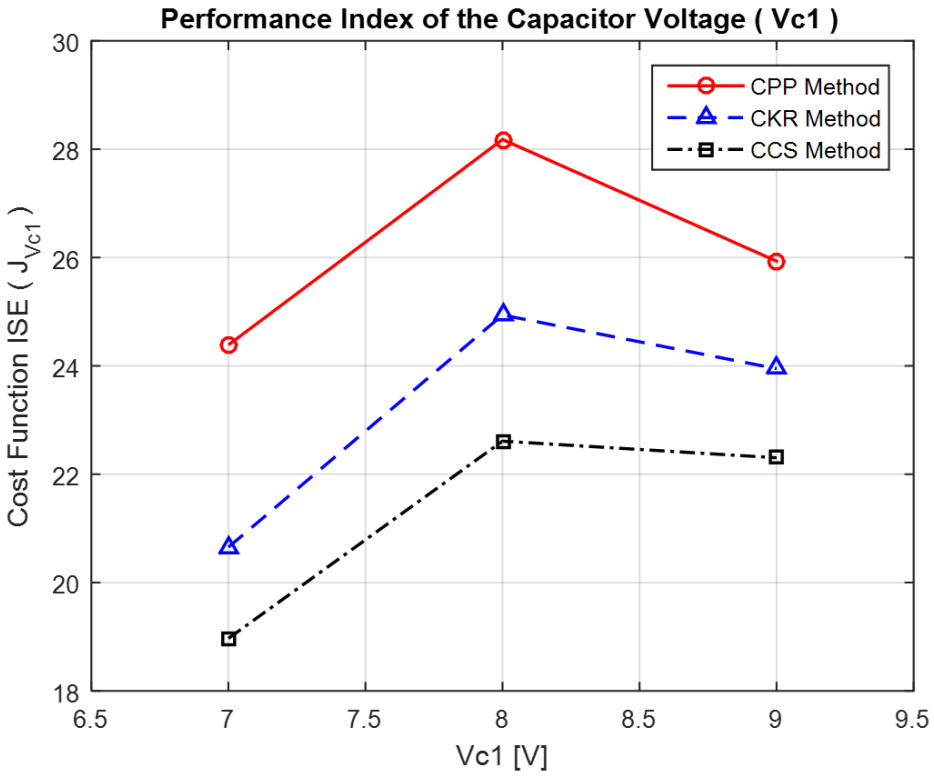

Figure 5.6. The cost function ISE of the experimental data collected system when the source converter is subjected to a reference voltage variation using a PID control structure.

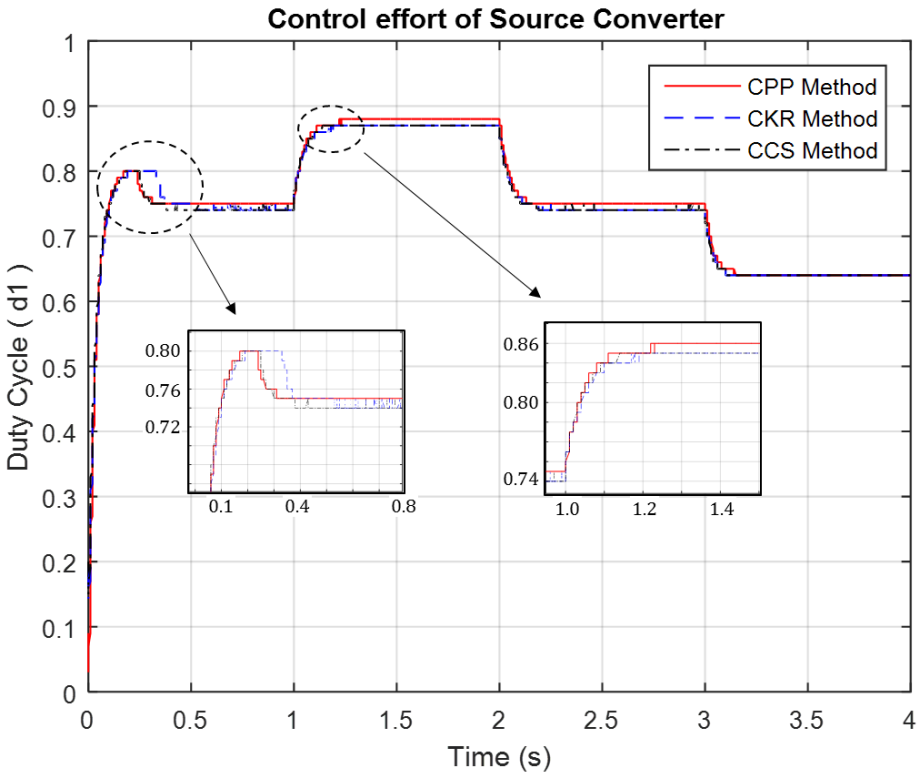

Figure 5.7. The experimental control effort test, when the source converter is subjected to a reference voltage variation using a PID control structure.

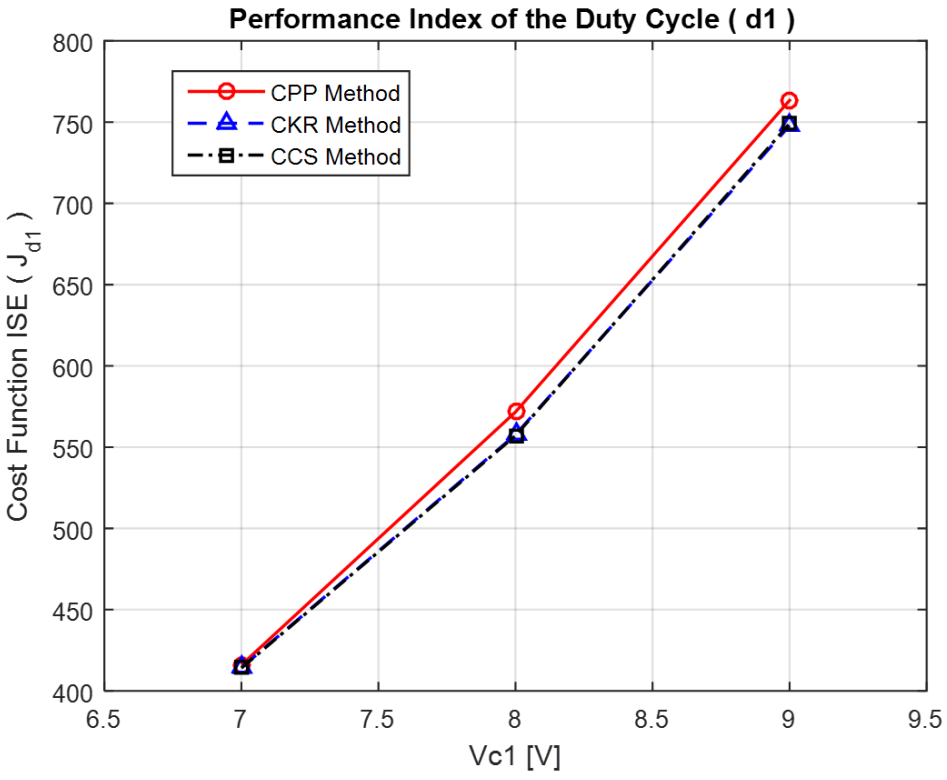

Figure 5.8. The cost function ISE of control effort of the experimental data collected when the source converter is subjected to a reference voltage variation using a PID control structure.

5.3 EVALUATION OF POWER MODE CONTROL OF LOAD CONVERTER

Aiming to develop a performance evaluation of the control methodology evaluated in this work, when the load converter is powered by a fixed voltage source of 8 V. A variation in reference power is performed as mentioned in subsection 4.5.2, in order to verify that the pre-established performance conditions of closed-loop system are fulfilled.

5.3.1 Simulation environment

The non-linear system is developed in Matlab/Simulink to evaluate the performance of control strategies applied to load converter in order to verify the robustness of the control strategies under variation of the reference power in a variation range of ± 0.1 p.u. of its operating point. Fig. 5.9 shows the result obtained from the non-linear simulation of the load converter controlled by a PID controller under variation of reference power.

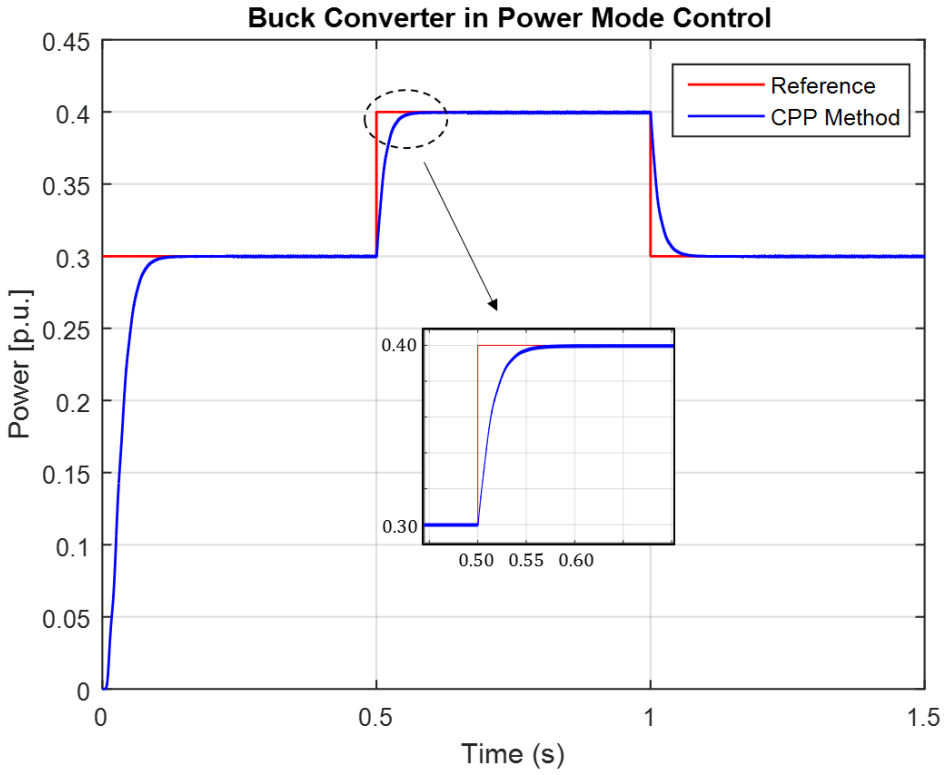

Figure 5.9. Simulated test of the load converter using a PID control structure when the system is subjected to a reference power variation.

Fig. 5.9 shows that the CPP method met the performance specifications in closed loop, tracking the reference for the entire range of its operating point variation. Fig. 5.10 shows the control effort by using a PID control structure.

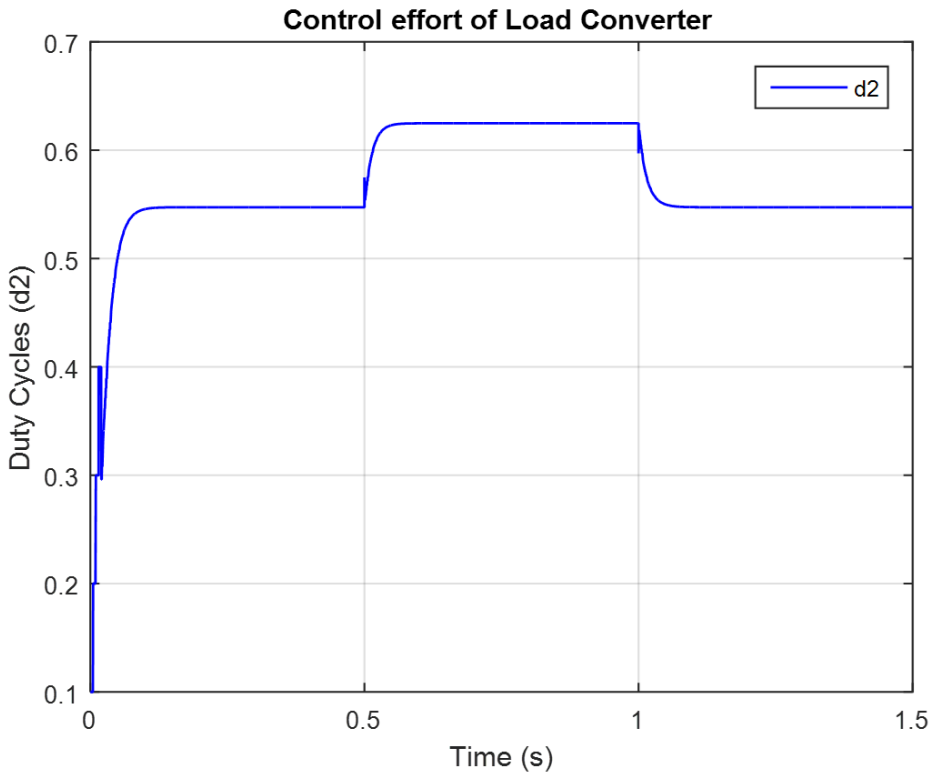

Figure 5.10. The simulated control effort test, when the load converter is subjected to a reference power variation using a PID control structure.

5.3.2 Experimental environment

Fig. 5.11 shows the experimental evaluation performed in the load converter, using a PID control structure, when the system is subjected to a reference power variation from 0.3 p.u. to 0.4 p.u., and then from 0.4 p.u. to 0.3 p.u. again, verifying that the closed-loop performance is fulfilled. The CPP methods has succeeded in tracking reference for the entire range of variation of its operating point. Fig. 5.12 shows the control effort by using a PID control structure.

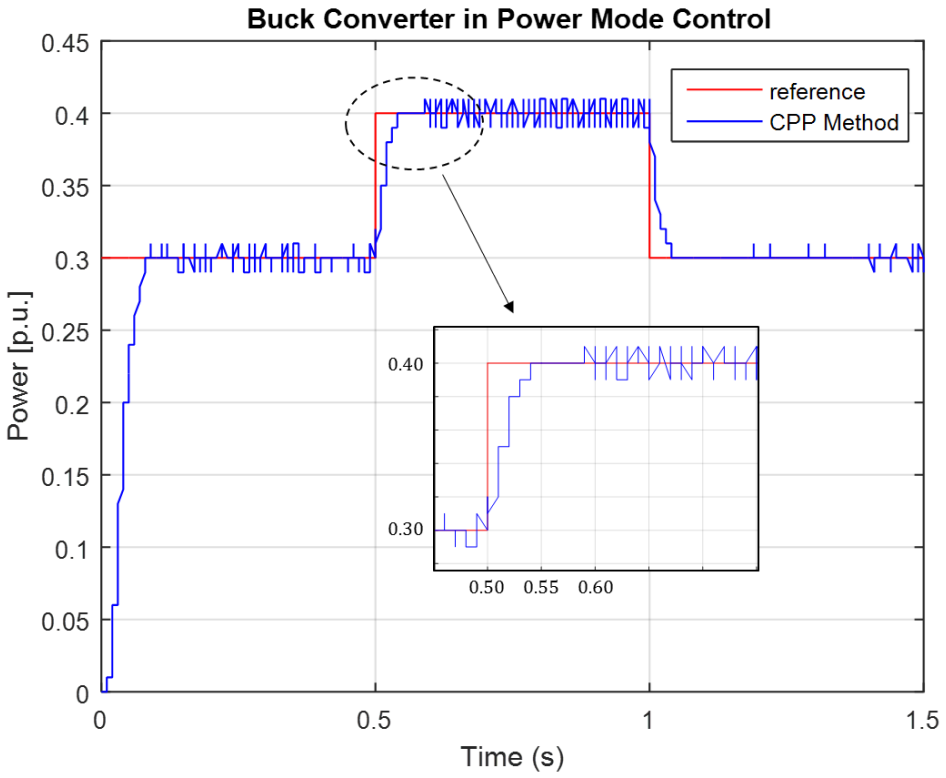

Figure 5.11. Experimental test of the load converter using a PID control structure when the system is subjected to a reference power variation.

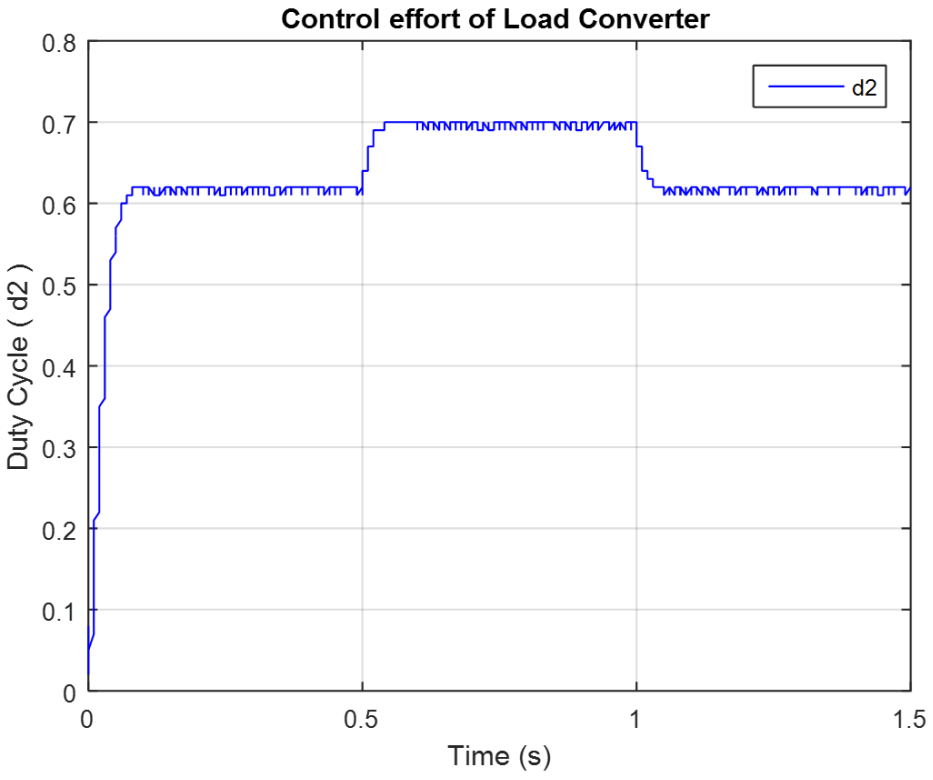

Figure 5.12. The experimental control effort test, when the load converter is subjected to a reference power variation using a PID control structure.

5.4 PERFORMANCE EVALUATION OF SOURCE CONVERTER FEEDING A CPL UNDER POSITIVE POWER VARIATION

Aiming to develop a performance evaluation of the control methodologies evaluated in this work, when the source converter is feeding the load converter, which acts as a CPL. In the multi-converter buck-buck system, the load converter is considering a load for the source converter. Therefore, any change in the operating conditions of load converter affects as a load disturbance at the output of the source converter. A positive power variation is considered in the following tests within of an operating range from 0.3 p.u. to 0.8 p.u for simulated and experimental tests, verifying that the closed-loop performance of the multi-converter buck-buck system is fulfilled.

5.4.1 Simulation environment

The non-linear system is developed in Matlab/Simulink to evaluate the performance of control strategies applied to multi-converter buck-buck system, in order to verify the robustness of the control strategies under positive variation of the reference power. Fig. 5.13 shows the result obtained from the non-linear simulation of multi-converter buck-buck system controlled by PID controllers under positive variation of reference power. The source converter suffers four disturbances during the tests performed due to start operating with the load converter disconnected until it reaches its stable state at nominal operation point. Then the load converter is connected ($t = 0.5\ sec$) causing a load disturbance at the output voltage of source converter, so its output will leave from nominal operation point. Therefore, the voltage controller will correct oscillation due to load disturbance to guarantee reference tracking of output voltage of source converter. The next disturbance ($t = 1.0\ sec$) at the output of source converter is due to the change in the operating point of the load converter as shown in Fig 5.13.

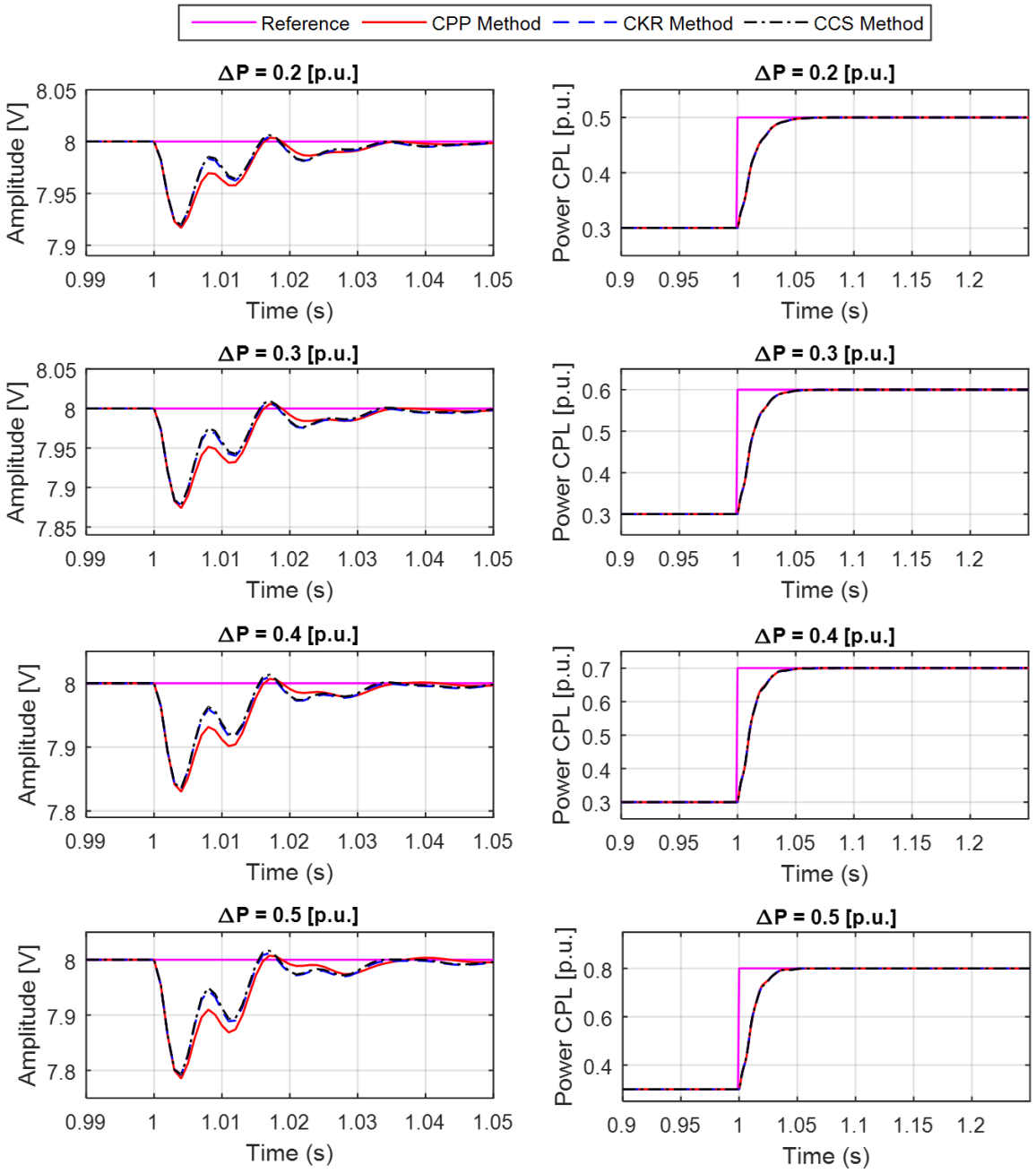

Figure 5.13. Simulated test of the multi-converter buck-buck system when the source converter is feeding a CPL using a PID control structures when the system is subjected to a positive variation of power reference.

Note that all control methods have succeeded in correcting the load disturbance at the output of source converter. However, the controller tuned by CCS method obtained a better ISE performance index than those obtained by CKR and CPP methods as shown in Fig. 5.14. Therefore, the impact of positive power variation is lower for the controller by CCS method. Fig 5.15 shows the ISE performance index at the output of load converter.

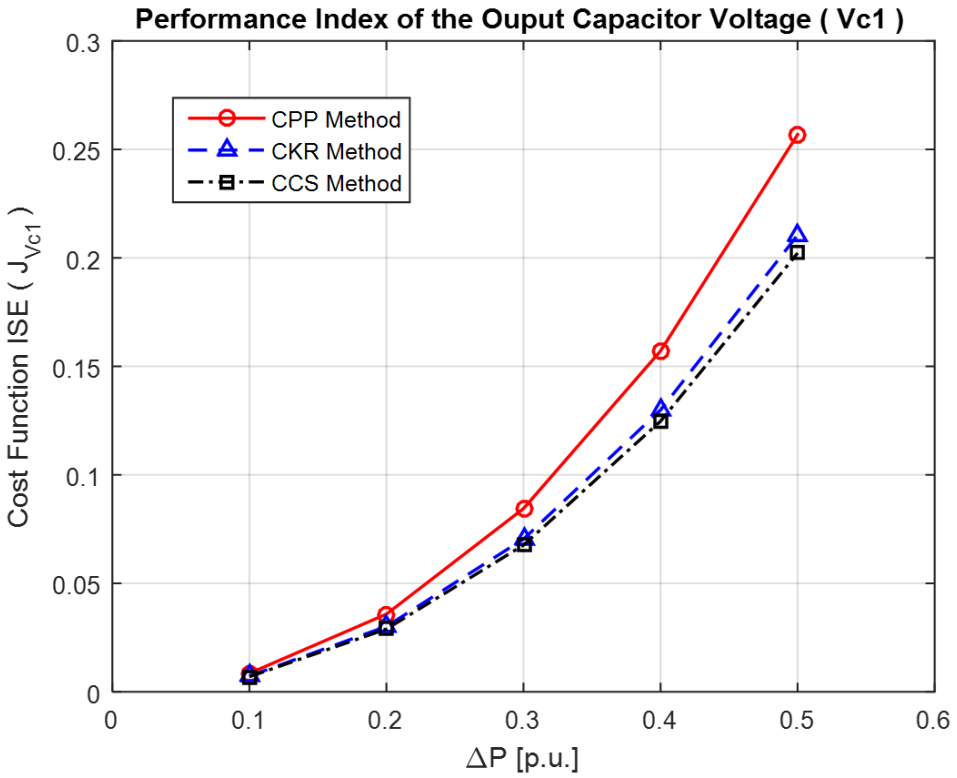

Figure 5.14. The simulated cost function ISE of source converter when multi-converter buck-buck system is subjected to a positive variation of power reference using a PID control structure.

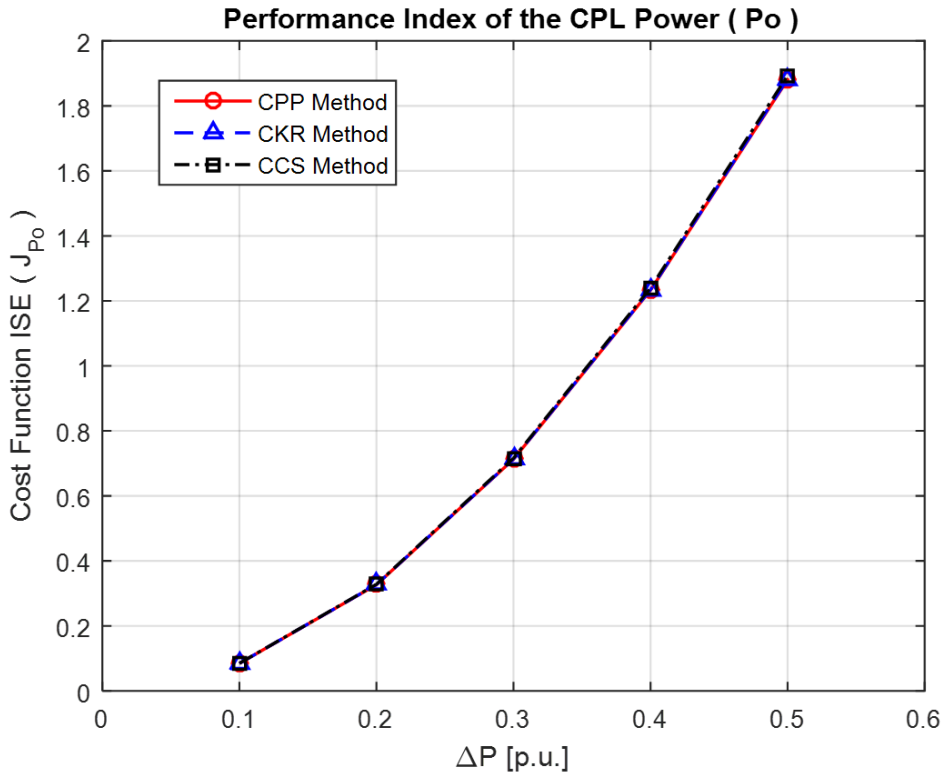

Figure 5.15. The simulated cost function ISE of load converter when multi-converter buck-buck system is subjected to a positive variation of power reference using a PID control structure.

Note that the performance of load converter does not deteriorate (see Fig. 5.15), even though there is a variation in the input source of load converter. Fig. 5.16 shows the control effort of multi-converter buck-buck system using a PID control structure. Note that all methods obtained a similar control effort as shown in the index performance. Fig. 5.17 shows the ISE index performance of control effort of voltage control of source converter. Fig. 5.18 shows the ISE index performance of control effort of power control for the different voltage control modes of source converter.

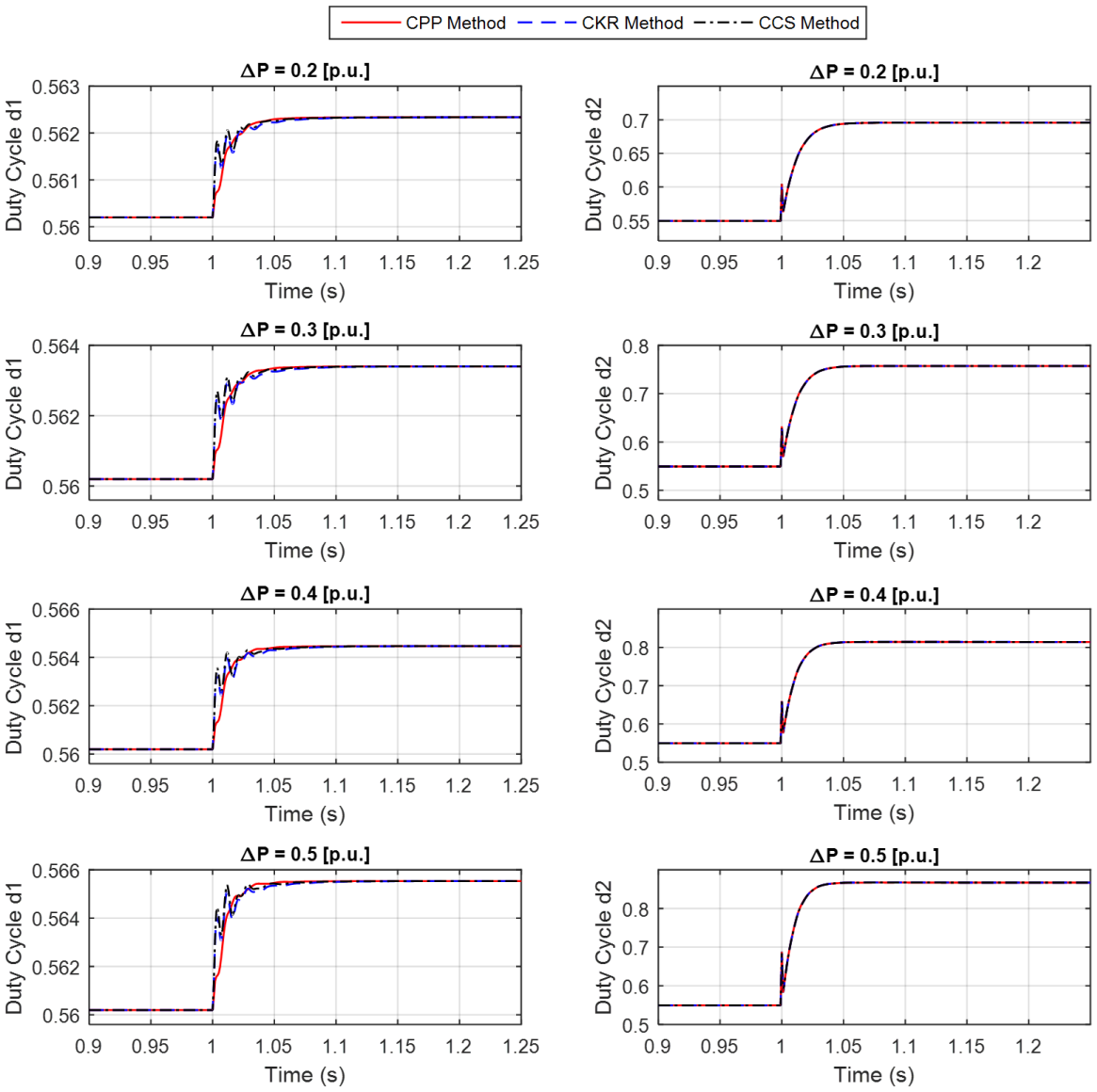

Figure 5.16. The control effort test of multi-converter buck-buck system, when the simulated system is subjected to a positive variation of power reference using a PID control structures.

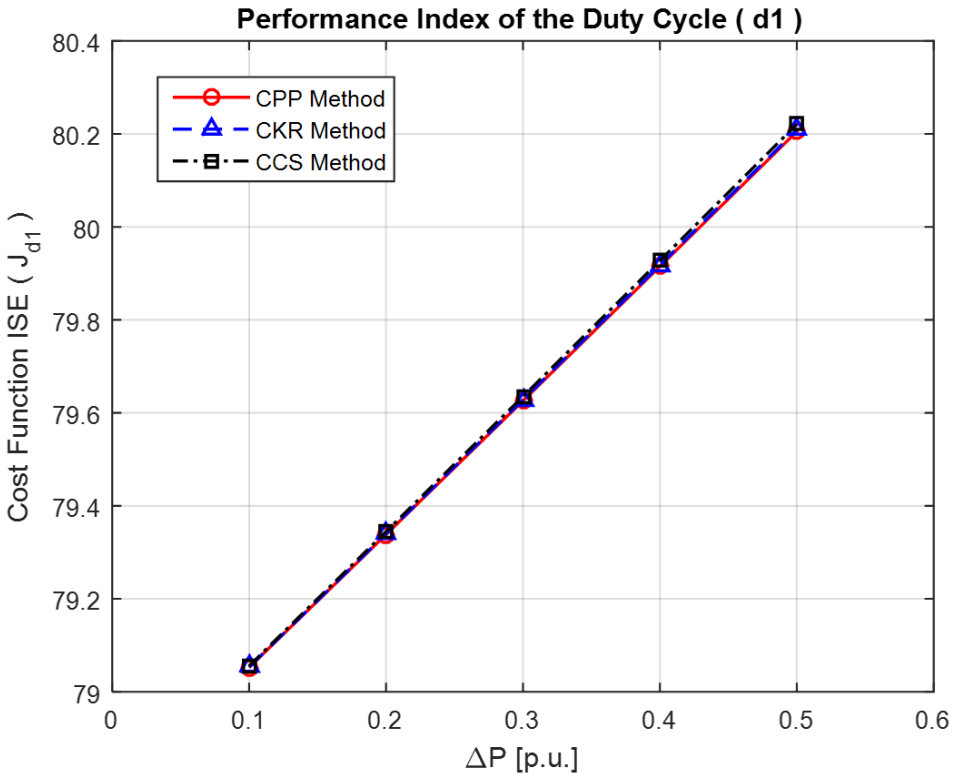

Figure 5.17. The cost function ISE of control effort of source converter when the simulated system is subjected to a positive variation of power reference using a PID control structure.

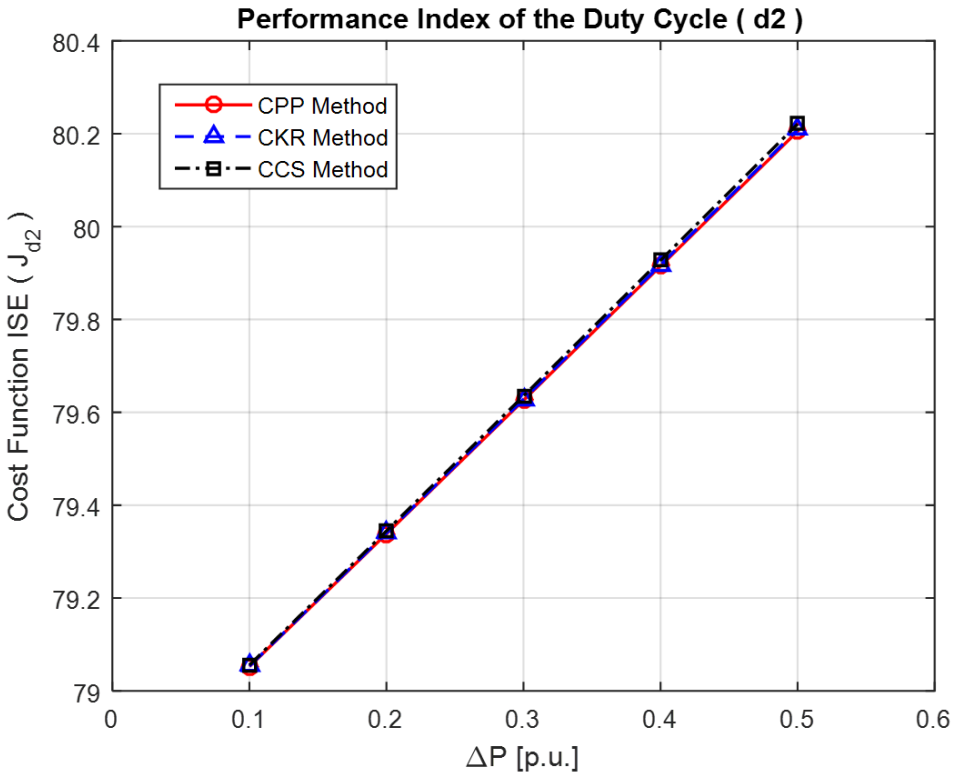

Figure 5.18. The cost function ISE of control effort of load converter when the simulated system is subjected to a positive variation of power reference using a PID control structure.

5.4.2 Experimental environment

The multi-converter buck-buck system stars with load converter disconnected until source converter achieves its steady state (see Table 4.3), then the load converter is connected ($t = 0.5\ sec$) causing a load disturbance at the output of source converter. When the multi-converter buck-buck system is operating in its steady state (8V and 0.3 p.u.), the system is subjected to a positive variation of power reference ($t = 1.0\ sec$) within an amplitudes range from 0.2 to 0.5 [p.u.]. Fig. 5.19 shows the experimental evaluation performed in the multi-converter buck-buck system, using a PID control structure.

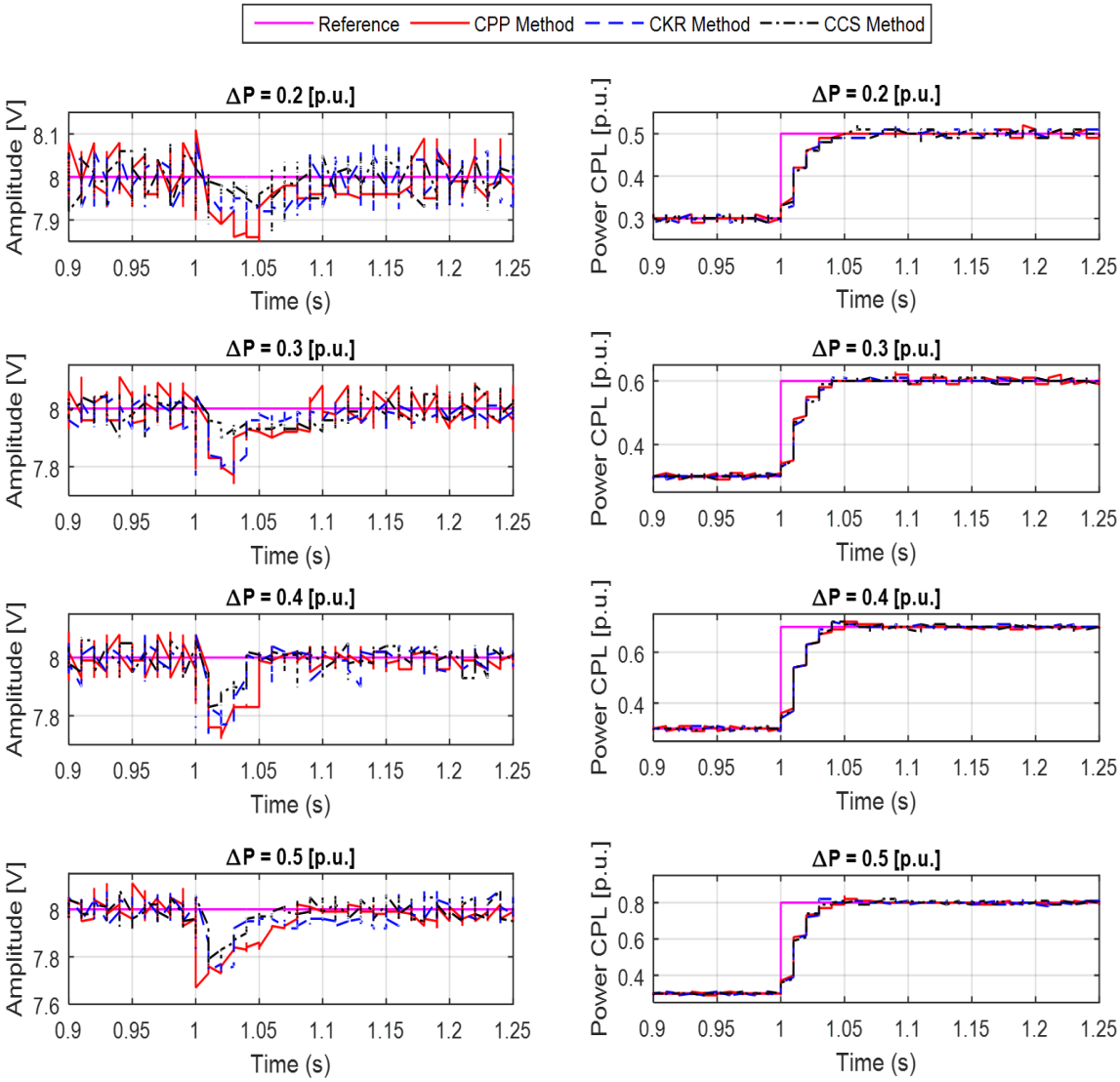

Figure 5.19. Experimental test of the multi-converter buck-buck system when the source converter is feeding a CPL using a PID control structures when the system is subjected to a positive variation of power reference.

Note that all control methods have succeeded in correcting the load disturbance at the output of source converter. However, the controller tuned by CCS method obtained a better ISE performance index than those obtained by CKR and CPP methods as shown in Fig. 5.20. Therefore, the impact of positive power variation is lower for the controller by CCS method. Although the controller of load converter does not change, different performances can be observed (see Fig. 5.19) due to the oscillation in the output voltage of source converter caused by the variation of power reference. Thereby, the controller of the voltage regulation stage that better compensates for the oscillations will cause less deterioration in the performance of the controller of the power control stage. Fig. 5.21 shows the ISE performance index of load converter when the multi-converter buck-buck system is subjected to a positive reference power variation using a PID control structures.

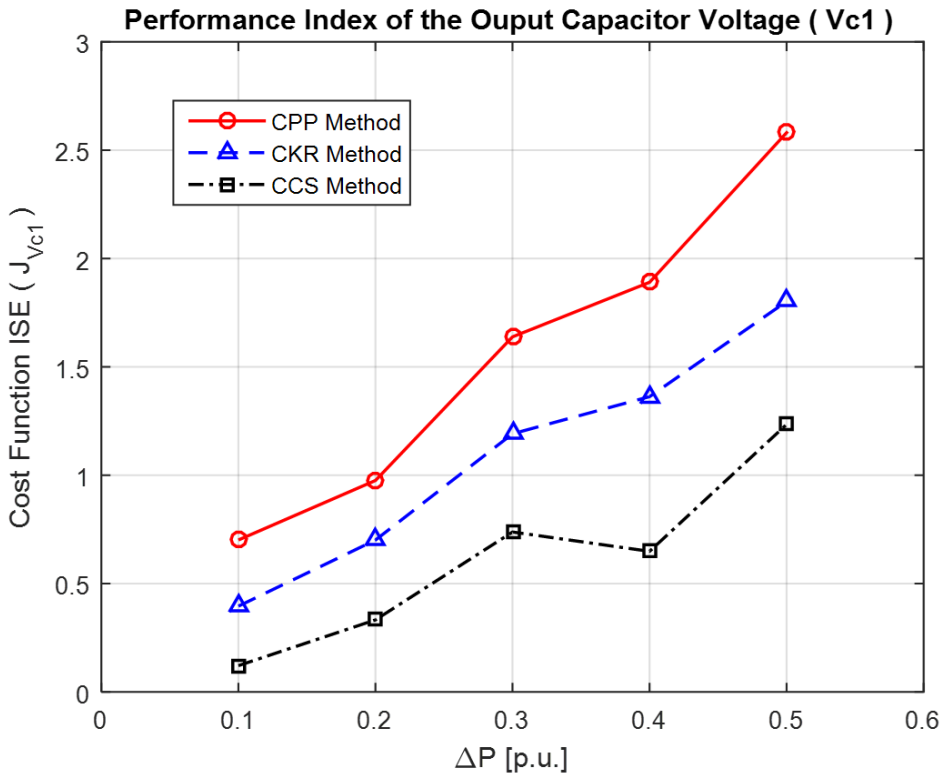

Figure 5.20. The experimental cost function ISE of source converter when multi-converter buck-buck system is subjected to a positive variation of power reference using a PID control structure.

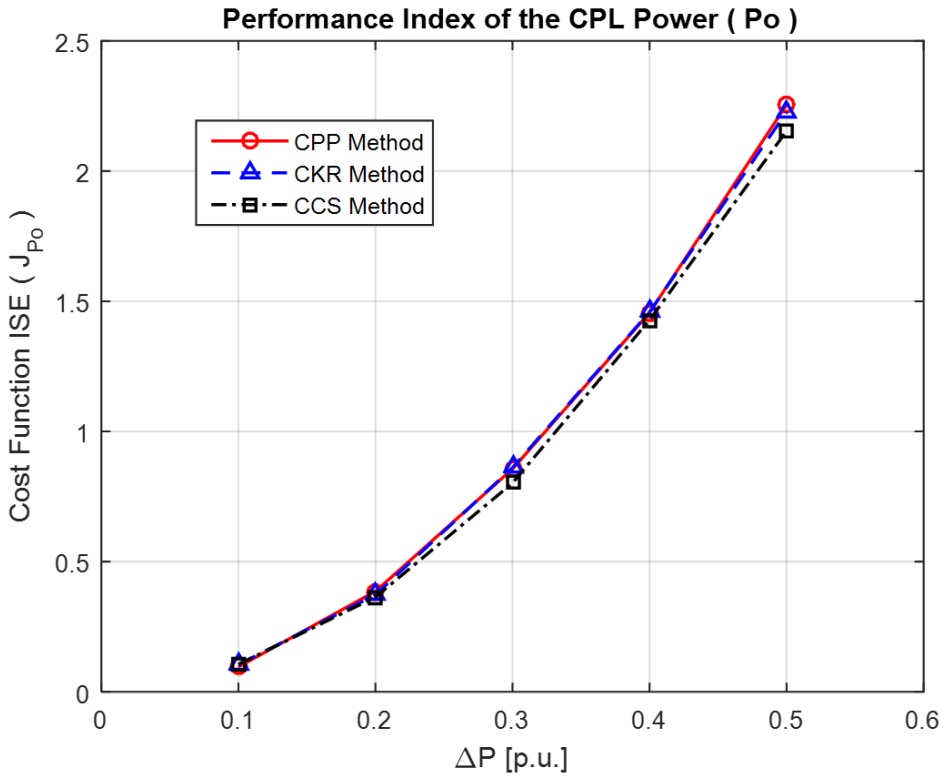

Figure 5.21. The experimental cost function ISE of load converter when multi-converter buck-buck system is subjected to a positive variation of power reference using a PID control structure.

Fig. 5.22 shows the control effort of multi-converter system, using a PID control structures for the experimental test noting that the saturation of the control signal does not occur at any time. Fig. 5.23 shows the ISE index performance of control effort of voltage control of source converter for the experimental test using a PID control structure. Fig. 5.24 shows the ISE performance index of load converter using a PID control structure. The control effort of system is lower when the voltage regulation stage is controlled by the RPC methods. This experimental result confirms the result obtained by simulation, demonstrating that for the majority variations evaluated by this experiment, the controllers designed by the RPC methodologies have a better performance, ratifying the robustness of the controller.

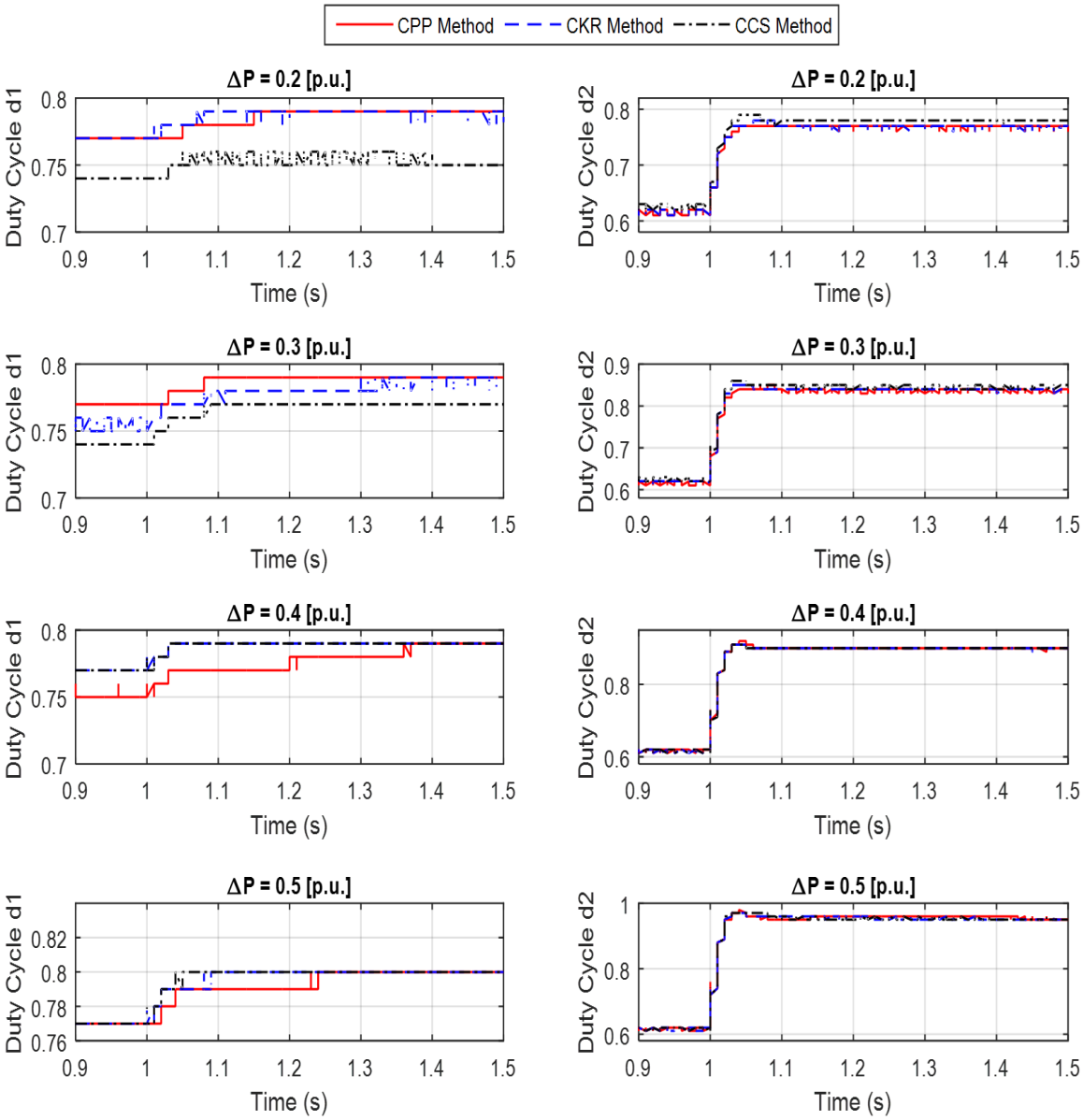

Figure 5.22. The control effort test of multi-converter buck-buck system, when the system is subjected to a positive variation of power reference using a PID control structures.

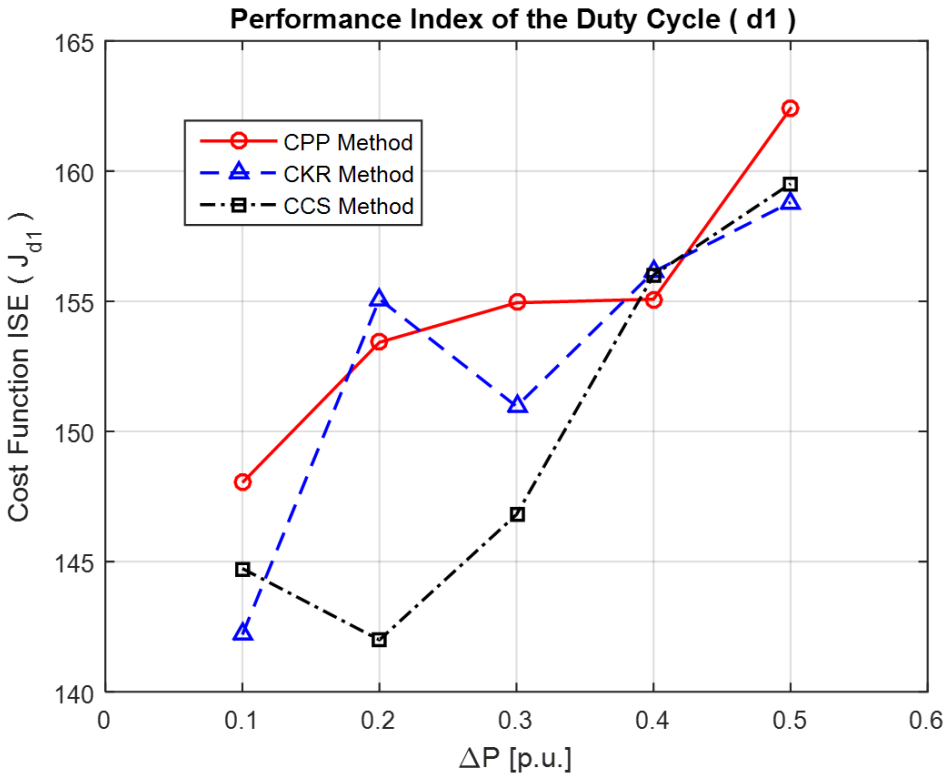

Figure 5.23. The cost function ISE of control effort of source converter when the experimental system is subjected to a positive variation of power reference using a PID control structure.

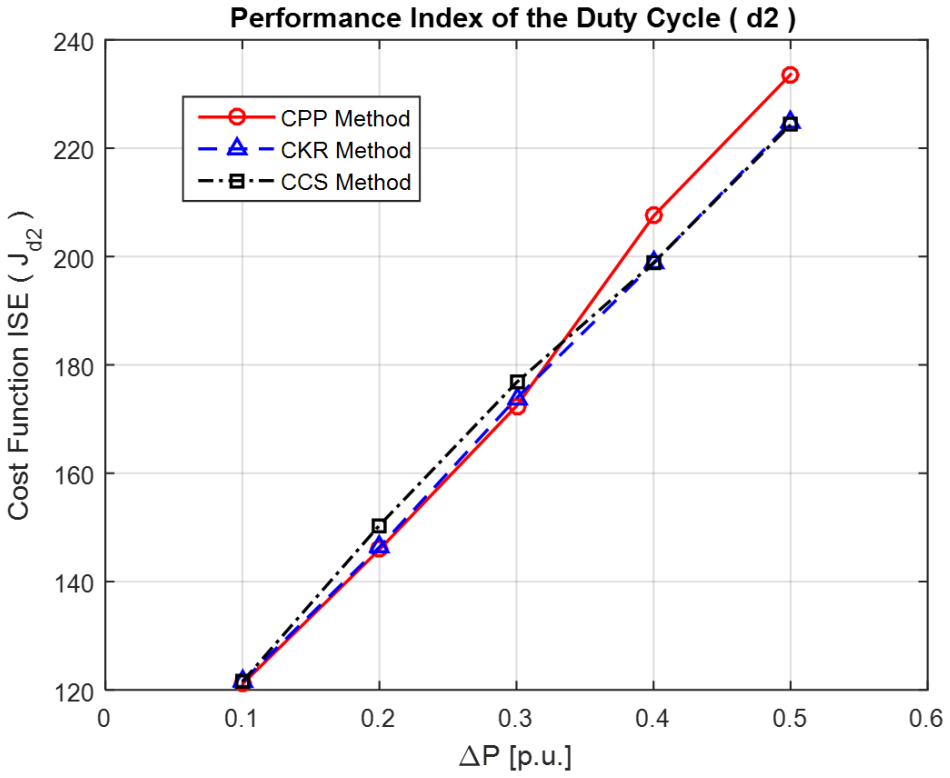

Figure 5.24. The cost function ISE of control effort of load converter when the experimental system is subjected to a positive variation of power reference using a PID control structure.

5.5 PERFORMANCE EVALUATION OF SOURCE CONVERTER FEEDING A CPL UNDER NEGATIVE POWER VARIATION

Aiming to develop a performance evaluation of the control methodologies evaluated in this work, when the load converter is feeding the source converter, which acts as a CPL. In the multi-converter buck-buck system, the load converter is considering a load for the source converter. Therefore, any change in the operating conditions of load converter affects as a load disturbance at the output of the source converter. A negative power variation is considered in the following tests within of a magnitude range of 0.2 p.u. to 0.7 p.u for simulated and experimental tests, verifying that the closed-loop performance of the multi-converter buck-buck system is fulfilled.

5.5.1 Simulation environment

The non-linear system is developed in Matlab/Simulink to evaluate the performance of control strategies applied to multi-converter buck-buck system, in order to verify the robustness of the control strategies under positive variation of the reference power. Fig. 5.25 shows the result obtained from the non-linear simulation of multi-converter buck-buck system controlled by PID controllers under negative variation of reference power. The source converter suffers four disturbances during the tests performed due to start operating with the load converter disconnected until it reaches its stable state at nominal operation point. Then the load converter is connected ($t = 0.5\ s$) causing a load disturbance at the output voltage of source converter, so its output will leave from nominal operation point. When the multi-converter buck-buck system is operating with the following conditions 8V and 0.7 p.u., the system is subjected to a negative variation of power reference ($t = 1.5\ seg$) within an amplitudes range from 0.2 to 0.5 [p.u.], causing a disturbance at output of source converter are due to the change in the operating point of load converter (see Fig 5.25).

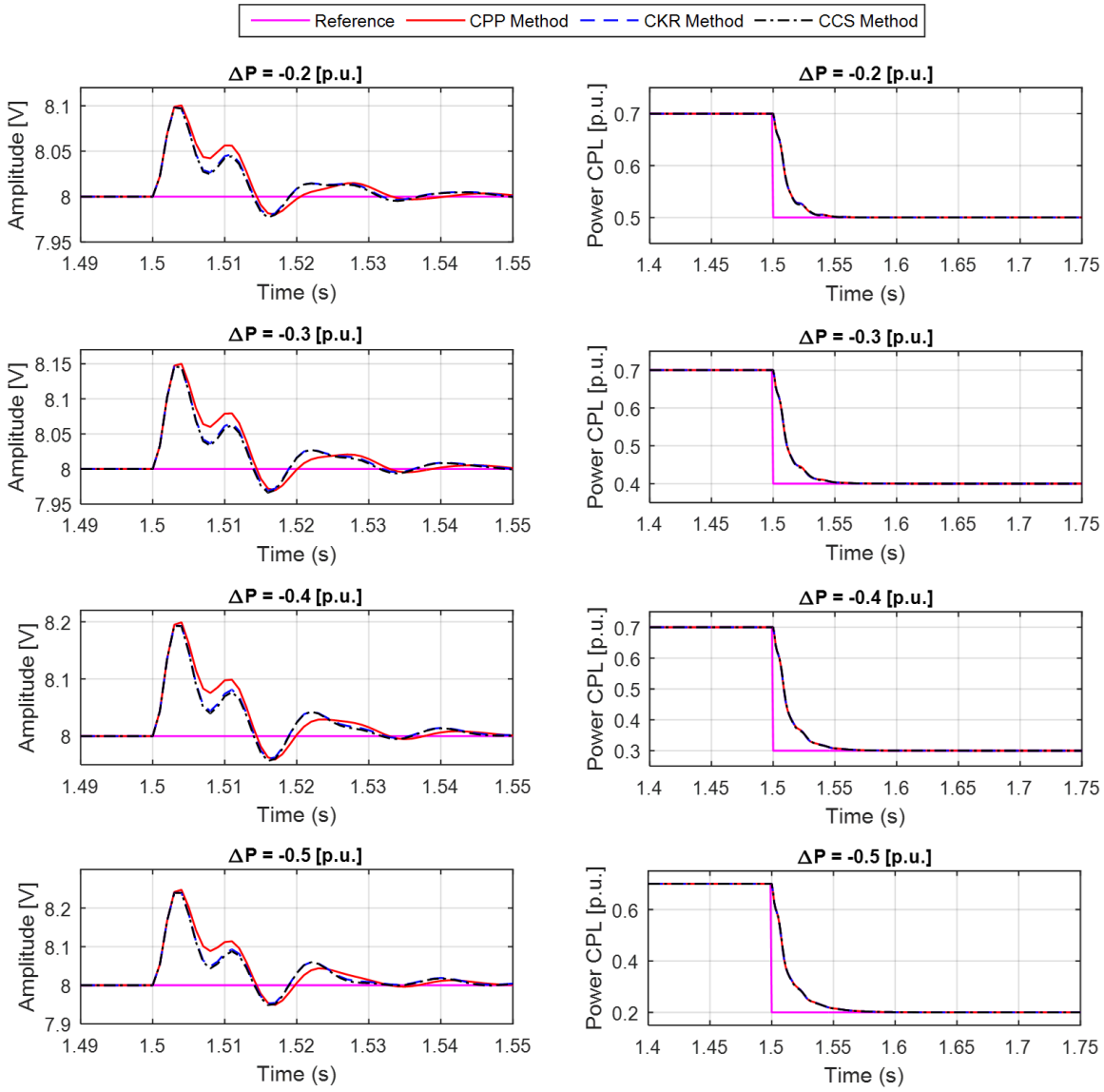

Figure 5.25. Simulated test of the source converter feeding a CPL using a PID control structure when the simulated system is subjected to a negative variation of power reference.

Note that all control methods have succeeded in correcting the load disturbance at the output of source converter. However, the controller tuned by CCS method obtained a better ISE performance index than those obtained by CKR and CPP methods as shown in Fig. 5.26. Therefore, the impact of positive power variation is lower for the controller by CCS method. Fig. 5.27 shows the ISE performance index at output of load converter.

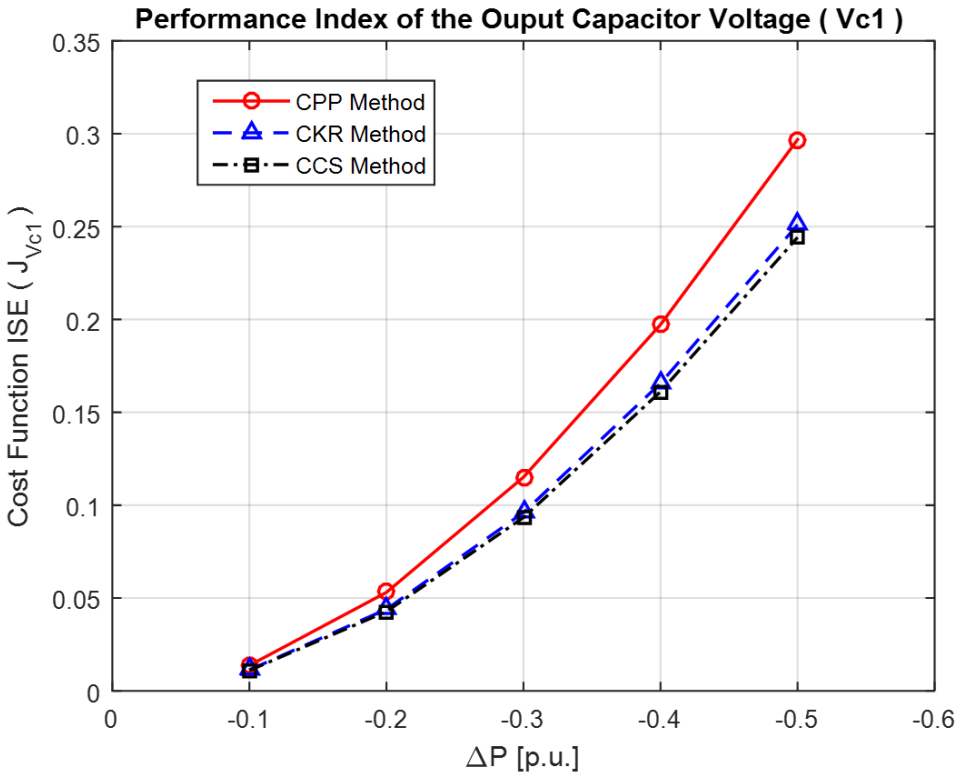

Figure 5.26. The simulated cost function ISE of source converter when multi-converter buck-buck system is subjected to a negative variation of power reference using PID control structure.

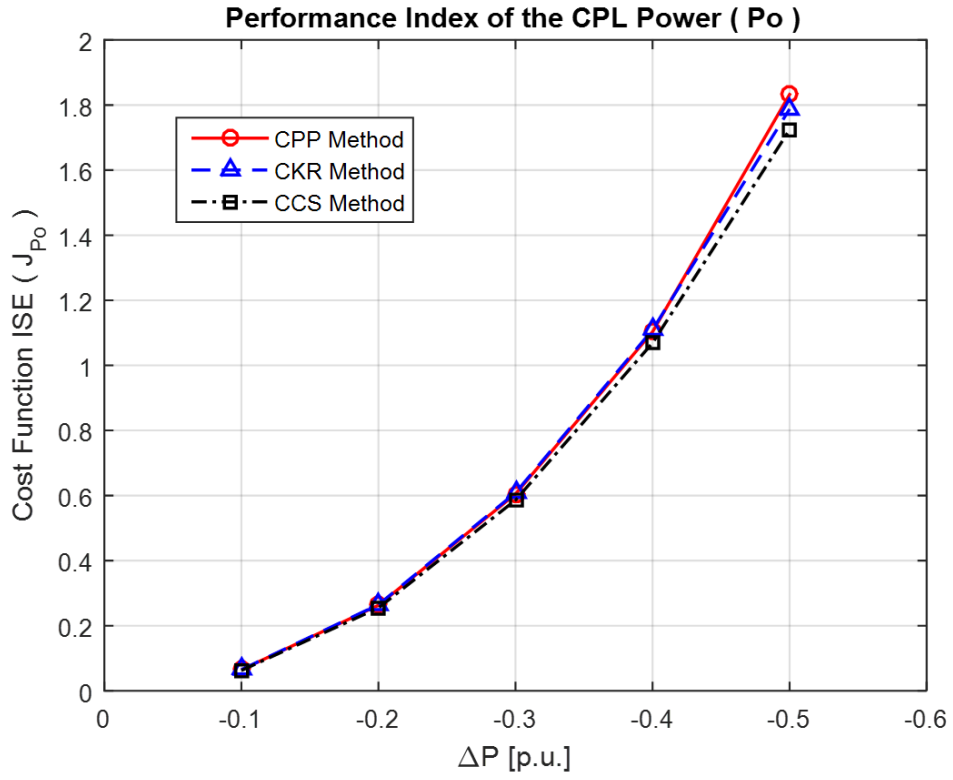

Figure 5.27. The simulated cost function ISE of control effort of load converter when simulated system is subjected to a negative variation of power reference using a PID control structure.

Although the power control of the load converter does not change, there are differences in performance (see Fig. 5.27) depending on the control strategy used in the voltage control of the source converter. Fig. 5.28 shows the control effort of multi-converter buck-buck system using a PID control structure. Note that all methods obtained a similar control effort as shown in the index performance. Fig. 5.29 shows the ISE index performance of control effort of voltage control of source converter. Fig. 5.30 shows the ISE index performance of control effort of power control for the different voltage control modes of source converter.

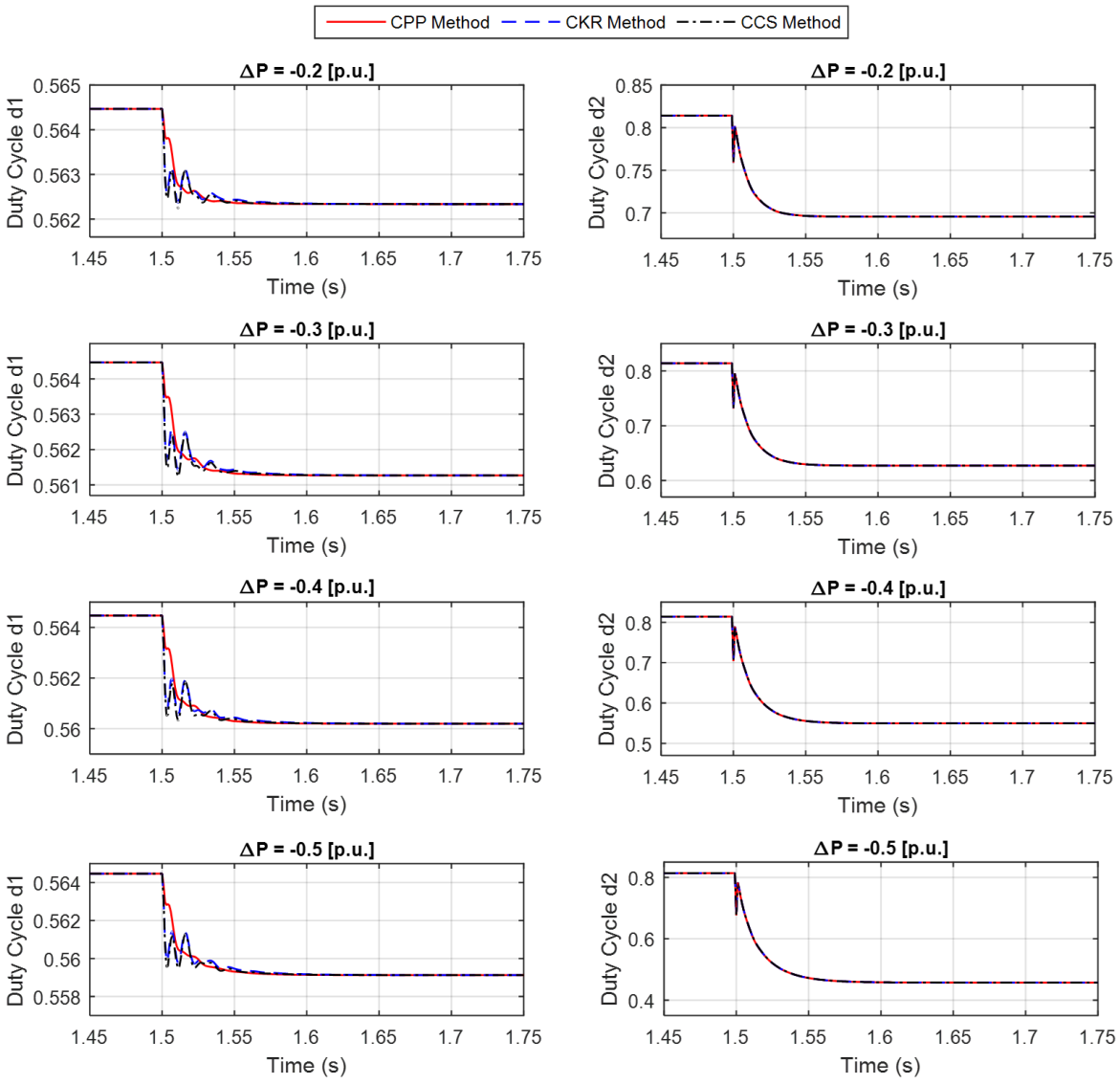

Figure 5.28. The control effort test of multi-converter buck-buck system, when the simulated system is subjected to a negative variation of power reference using a PID control structures.

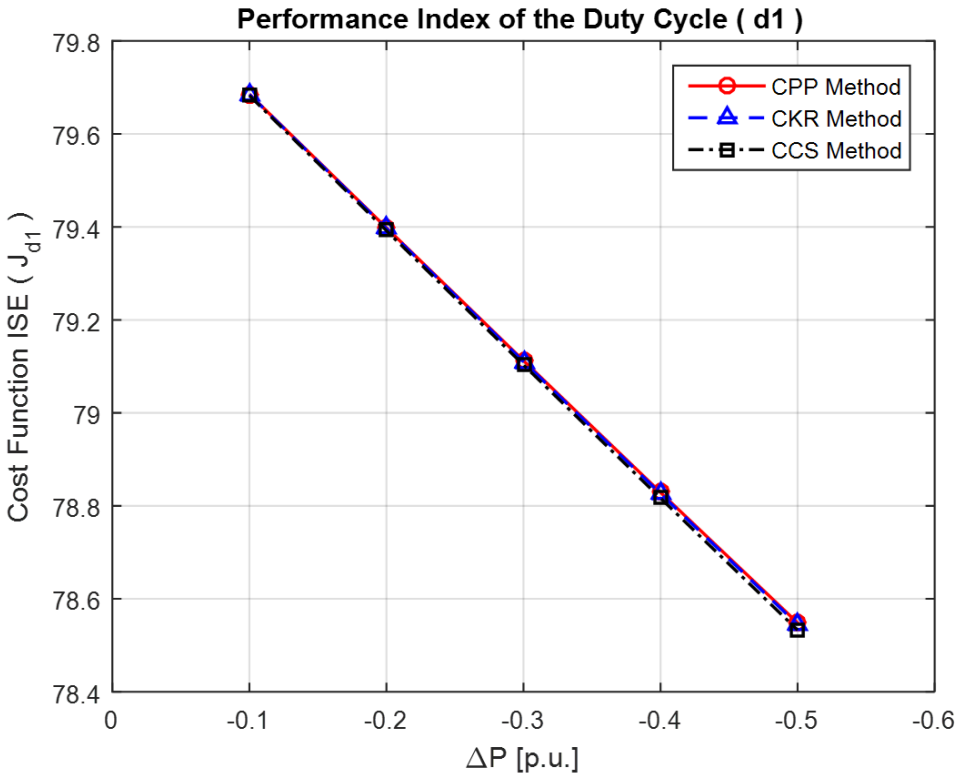

Figure 5.29. The cost function ISE of control effort of source converter when the simulated system is subjected to a negative variation of power reference using a PID control structure.

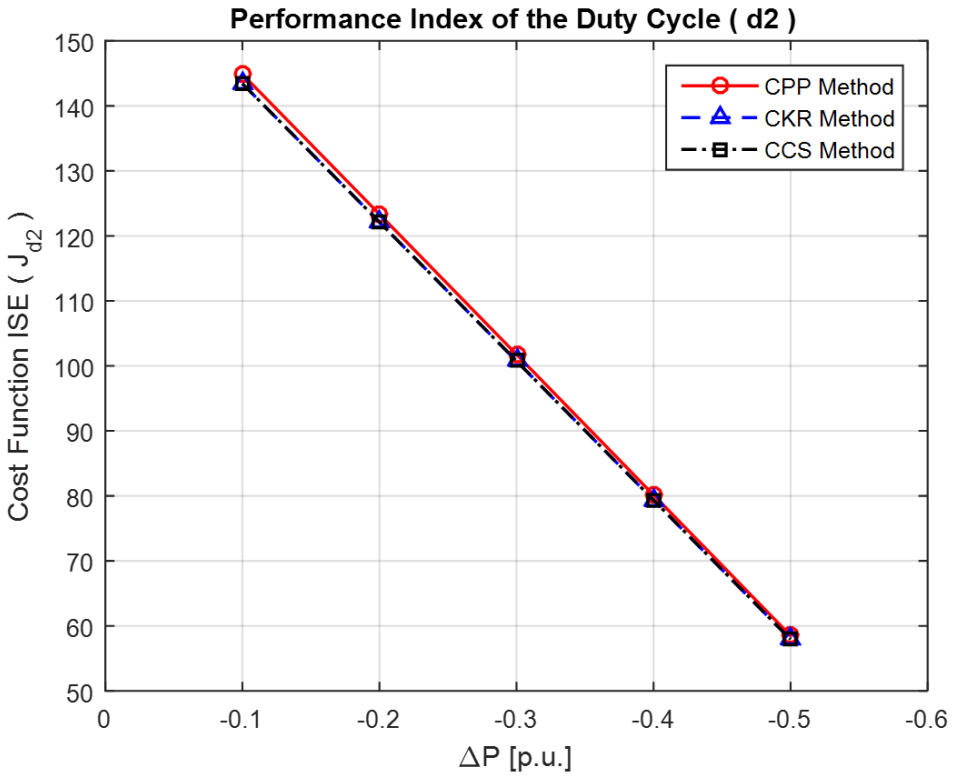

Figure 5.30. The cost function ISE of control effort of load converter when the simulated system is subjected to a negative variation of power reference using a PID control structure.

5.5.2 Experimental environment

The multi-converter buck-buck system stars with load converter disconnected until source converter achieves its steady state (see Table 4.3), then the load converter is connected ($t = 0.5\ seg$) causing a load disturbance at the output of source converter. When the multi-converter buck-buck system is operating with the following conditions 8V and 0.7 p.u., the system is subjected to a negative variation of power reference ($t = 1.5\ seg$) within an amplitudes range from 0.2 to 0.5 [p.u.]. Fig. 5.31 shows the experimental evaluation performed in the multi-converter buck-buck system, using a PID control structure.

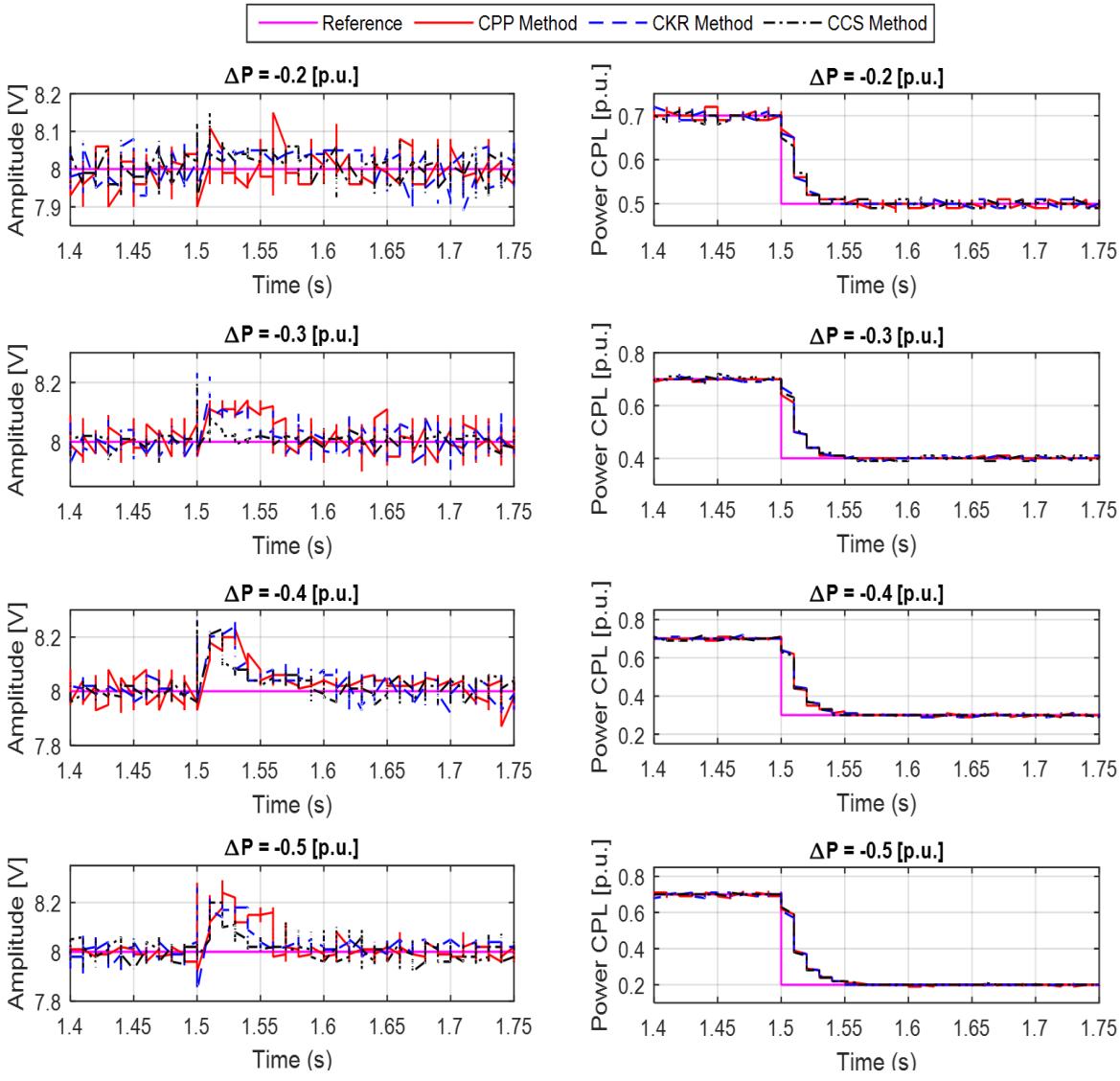

Figure 5.31. Experimental test of the source converter feeding a CPL using a PID control structure when the system is subjected to a negative reference power variation.

Note that all control methods have succeeded in correcting the load disturbance at the output of source converter. However, the controller tuned by CCS method obtained a better ISE performance index than those obtained by CKR and CPP methods as shown in Fig. 5.32. Therefore, the impact of negative power variation is lower for the controller by CCS method. Although the controller of load converter does not change, different performances can be observed (see Fig. 5.33) due to the oscillation in the output voltage of source converter caused by the variation of power reference. Thereby, the controller of the voltage regulation stage that better compensates for the oscillations will cause less deterioration in the performance of the controller of the power control stage. Fig. 5.33 shows the ISE performance index of load converter when the multi-converter buck-buck system is subjected to a negative variation of power reference using a PID control structures.

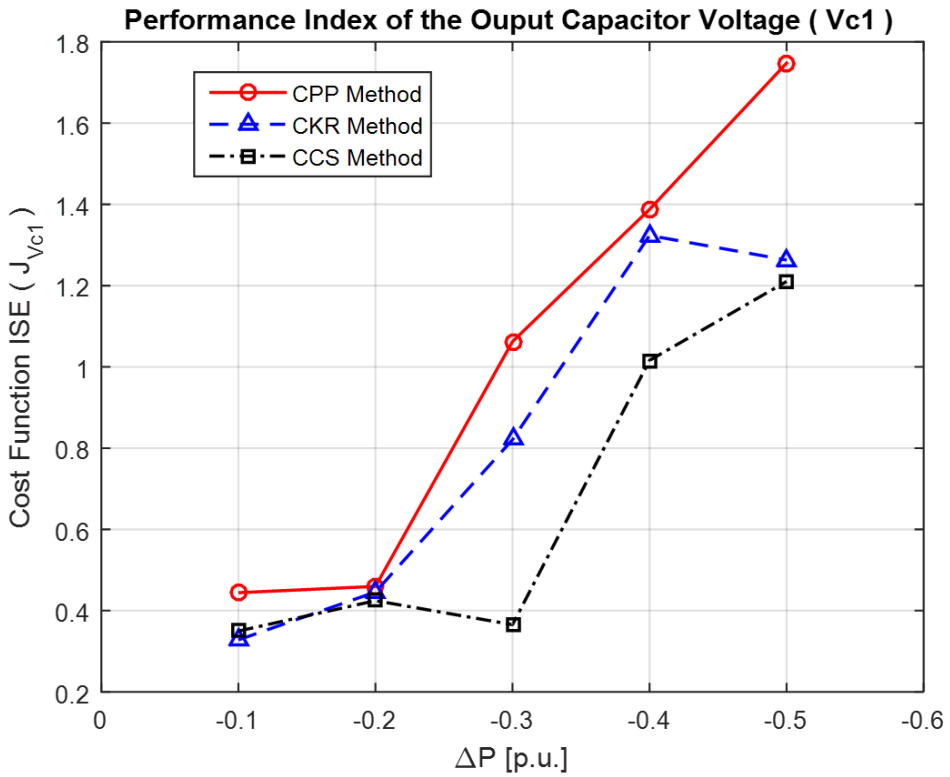

Figure 5.32. The cost function ISE of source converter when the multi-converter buck-buck system is subjected to a negative reference power variation using a PID control structure.

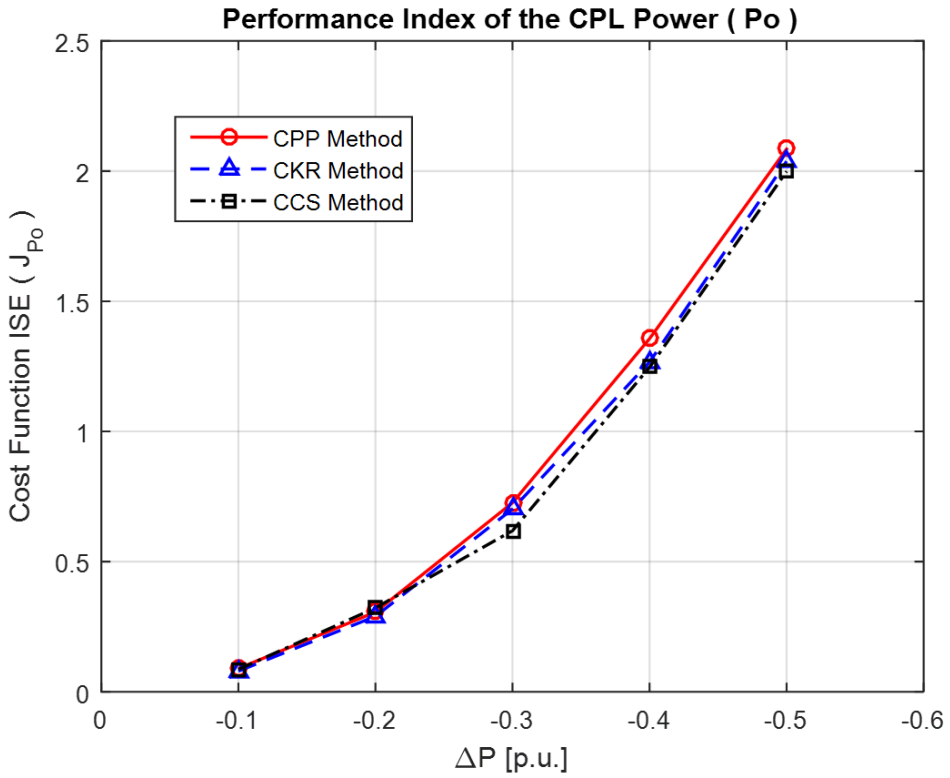

Figure 5.33. The cost function ISE of load converter when the multi-converter buck-buck system is subjected to a negative reference power variation using a PID control structure.

Fig. 5.34 shows the control effort of multi-converter system, using a PID control structures for the experimental test noting that the saturation of the control signal does not occur at any time. Fig. 5.35 shows the ISE index performance of control effort of voltage control of source converter for the experimental test using a PID control structure. Fig. 5.36 shows the ISE performance index of load converter using a PID control structure when the system is subjected to negative variation of power reference. The control effort of system is lower when the voltage regulation stage is controlled by the RPC methods. This experimental result confirms the result obtained by simulation, demonstrating that for the majority variations evaluated by this experiment, the controllers designed by the RPC methodologies have a better performance, ratifying the robustness of the controller.

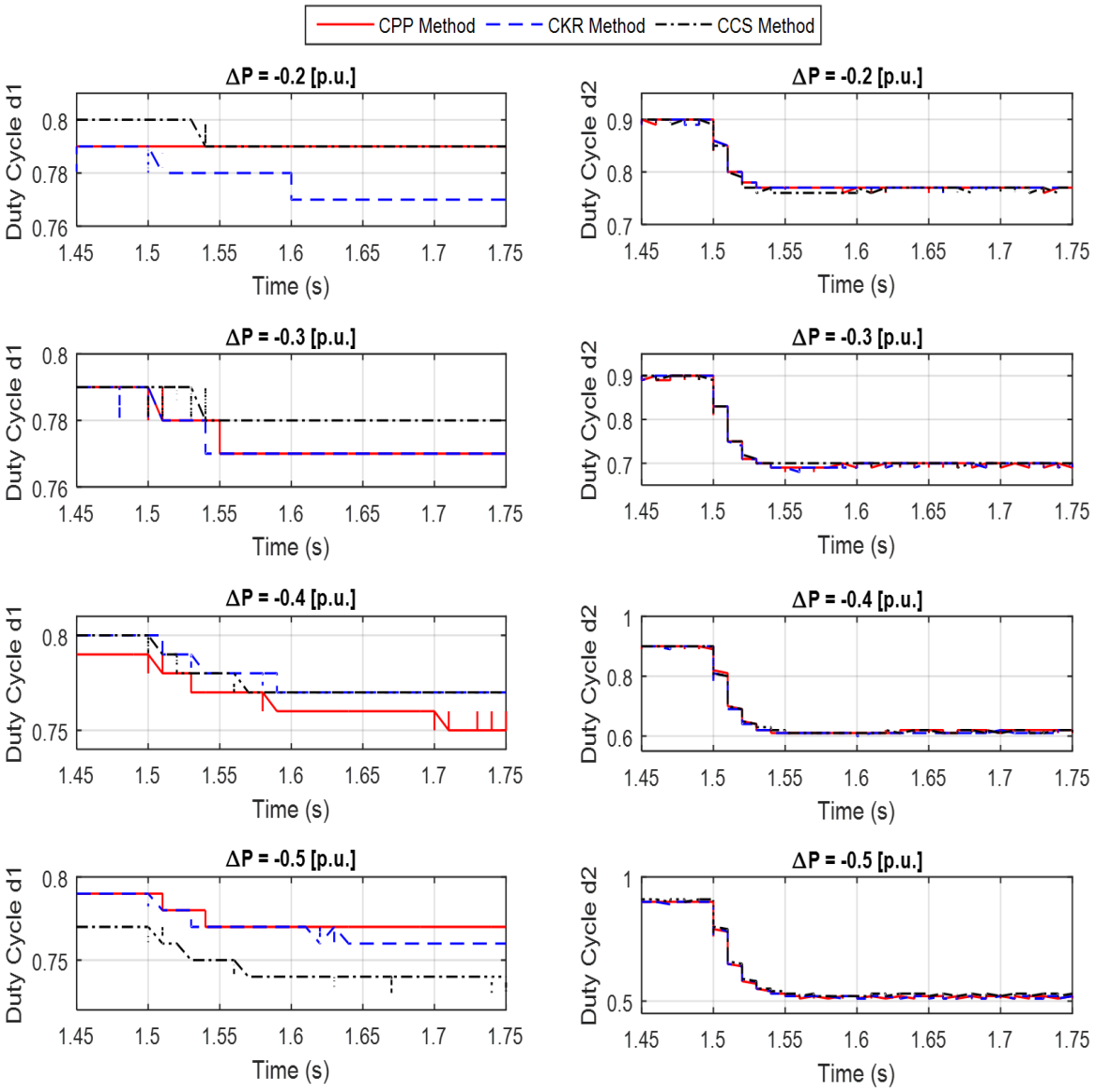

Figure 5.34. The control effort test of multi-converter buck-buck system, when the system is subjected to a positive reference power variation using a PID control structures.

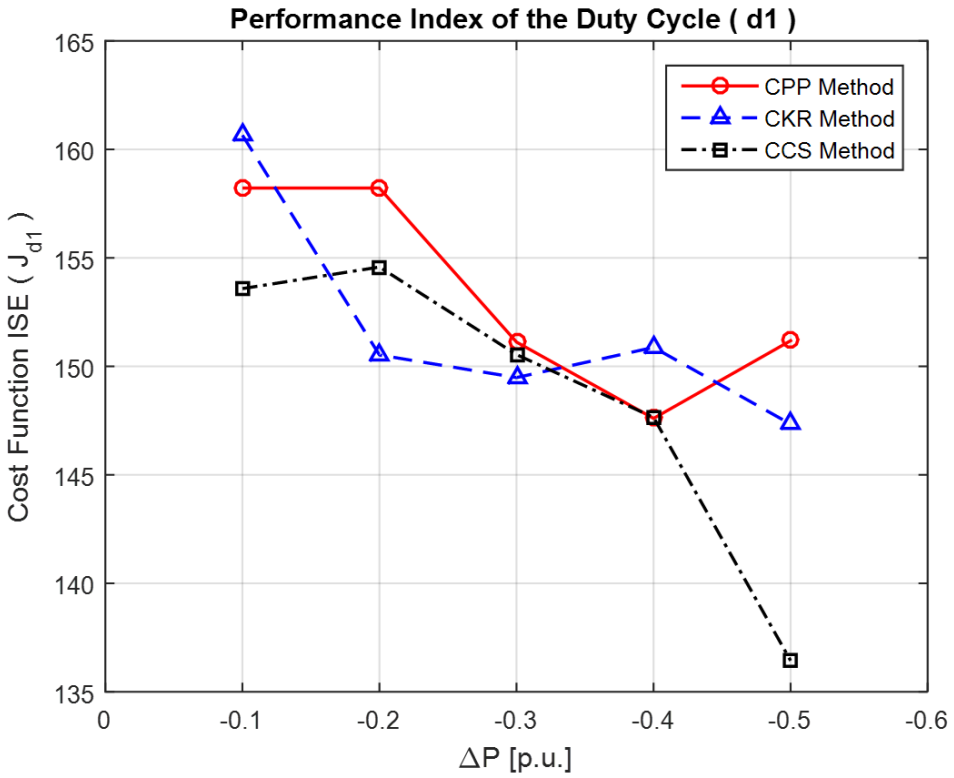

Figure 5.35. The cost function ISE of control effort of source converter when the system is subjected to a negative reference power variation using a PID control structure.

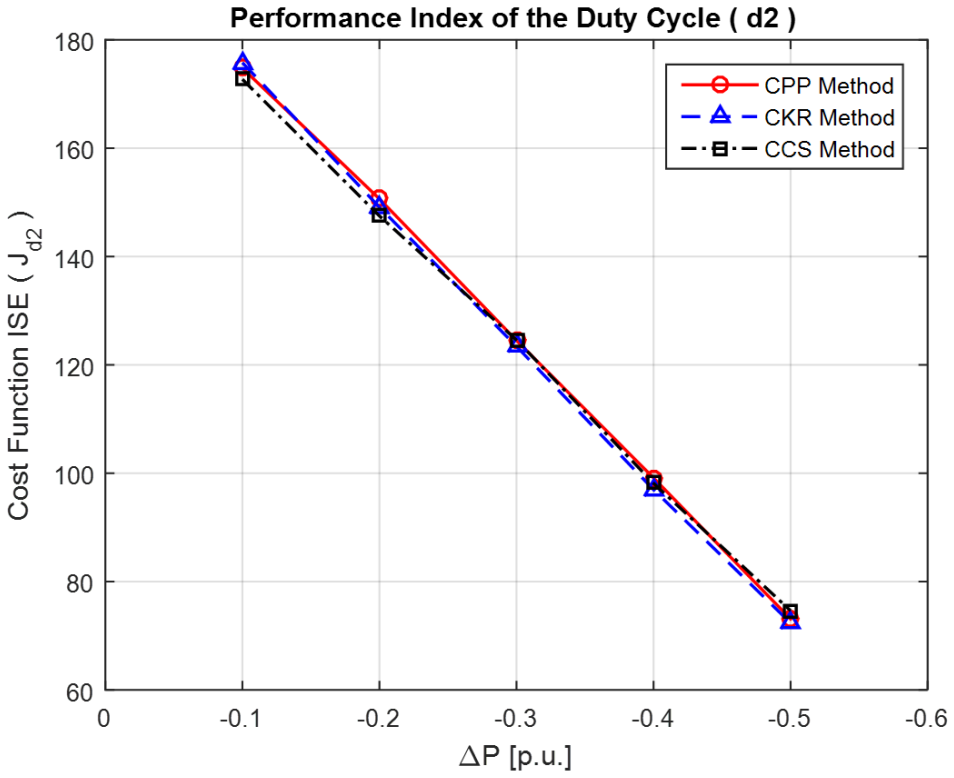

Figure 5.36. The cost function ISE of control effort of load converter when the system is subjected to a negative reference power variation using a PID control structure.

5.6 CONCLUSION OF THE CHAPTER

In this chapter, the results obtained by this study were presented; comparing the results of non-linear simulations and experimental tests by using PID controllers designed by CPP, CKR and CCS methods applied to multi-converter buck-buck system. In addition, the performance indicators presented by the controllers were evaluated resulting the CCS method as the best controller performance when the multi-converter system is subjected to a reference power variation in comparison with CPP and CKR methods. The next chapter deals with the final considerations of this study, besides the proposals of the future works.

CHAPTER 6

FINAL CONSIDERATIONS OF THE DISSERTATION AND RECOMMENDATIONS FOR FUTURE WORKS

6.1 FINAL CONSIDERATIONS

In this study, Robust Parametric Control strategies is proposed to control the output voltage of source converter when the multi-converter buck-buck system is subjected to reference power variation verifying that the robust parametric control methodologies (CKR and CCS) presented an excellent performance in comparison to the conventional methodology (CPP). By the study developed, it was verified that the load converter acts as a CPL when it is tightly regulated, its switching operation frequency and its dynamic response is faster than source converter in a multi-converter buck-buck system becoming the control design a problem of difficult solution.

According to the results obtained via simulation and experimentally, it is concluded that when the multi-converter buck-buck system is subjected to a certain reference power variation, the CCS method more effectively compensates the oscillations of output voltage of source converter improving the performance of the whole system because it also improves the performance of the load converter.

One of the main relevant contributions of this work is the design of interval robust controllers, applied to the control of a DC power buck converter feeding a constant power load, previously considering a certain region of uncertainties known by the designer. To the best of the author knowledge, in the literature, there is no control research applied to the multi-converter system, which uses of robust parametric control techniques, where this work is developed, aiming to contribute through this proposed solution to instability problem caused by a CPL in a multi-converter system.

The general purpose of this work was achieved satisfactorily, because results obtained by simulation and experimentally of the multi-converter buck-buck system show that the control based on Chebyshev's Sphere to solve the LMI problem leads to better performance indexes than other approaches if the multi-converter buck-buck system is subjected to a reference power variation. Therefore, the main and specific objectives proposed by this study were achieved satisfactorily.

6.2 RECOMMENDATIONS FOR FUTURE WORKS

1) To design the power control of the load converter using robust parametric control methodologies considering a range of the parameter uncertainties of load converter.
2) To apply stochastic control techniques in order to decrease the deterioration of system performance caused by measurement noise.
3) To investigate alternative methodologies applied on suppression of oscillation in micro grid due variation on load in CPL.

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